Buck-Boost SOC with PD2.0/PD3.1/PPS Protocol

1 Features

- **Synchronous-Rectified Buck-Boost converter**
  - ✧ Input voltage range: 5V~30V
  - ✧ Integrated Buck-Boost power NMOS
  - ✧ Maximum output power: 45W
  - ✧ Support CV/CC output mode
- **USB-C and PD protocol**
  - ✧ Support 5V/9V/12V/15V/20V output
  - ✧ Support PD2.0/PD3.1/PPS protocol for USB-C port
  - ✧ Support 3.3V-21V, 10mV/step PPS
  - ✧ Support E-Marker cable
- **Fast charge output**
  - ✧ Support BC1.2 and Apple protocol
  - ✧ Support PD2.0/PD3.1/PPS protocol
  - ✧ Support QC2.0/QC3.0/QC3.0+/QC4+/ QC5 protocol
  - ✧ Support FCP/HSCP protocol
  - ✧ Support AFC protocol
  - ✧ Support MTK protocol
  - ✧ Support UFCS protocol
- **Multi-protection and high reliability**
  - ✧ Support input OVP and UVP
  - ✧ Support output OVP, OCP and SCP
  - ✧ Over temperature protection
  - ✧ NTC Board-level temperature detection
  - ✧ ESD 4KV

2 Applications

- **Car Charger**

3 Description

IP6558 integrates a Synchronous-Rectified Buck-Boost converter and supports multiple fast charge output protocols, which provides complete solutions for car charger.

IP6558 needs one inductor to achieve charging solutions with Buck-Boost function, which can reduce overall solution size effectively.

IP6558 can provide maximum 45W (20V2.25A) output and supports NTC board-level temperature detection, which can intelligently adjust the output power according to the temperature.

IP6558 output supports CV/CC features, when the output current is lower than preset value, the output voltage will be constant in CV output mode; when the output current is higher than preset value, the output voltage will decrease as CC output mode.

IP6558 integrates with a variety of protection functions, including input over voltage, under voltage and output over current, over voltage, under voltage, short circuit protection.

IP6558 integrates 14-bit ADC to accurately measure the voltage and current of the input/output.

Package: QFNWB-7*7-60L 0.4pitch.

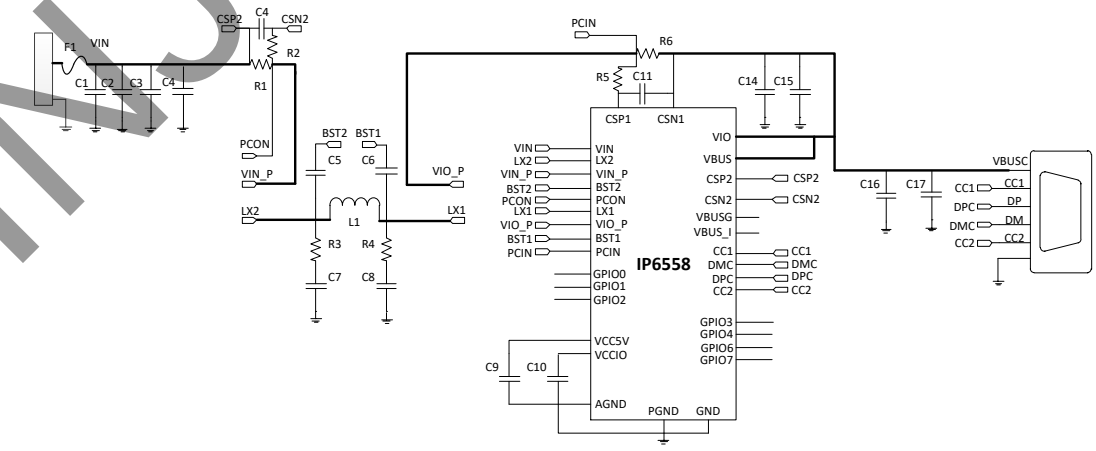


Figure 1 Simplified application schematic diagram of IP6558 single C port output

Contents

4 Revision History

Notes: The page number of the previous version may different from the page number of the current version.

Initial Release V 1.00 (Sept. 2024)

5 Simplified Application Schematic Diagram

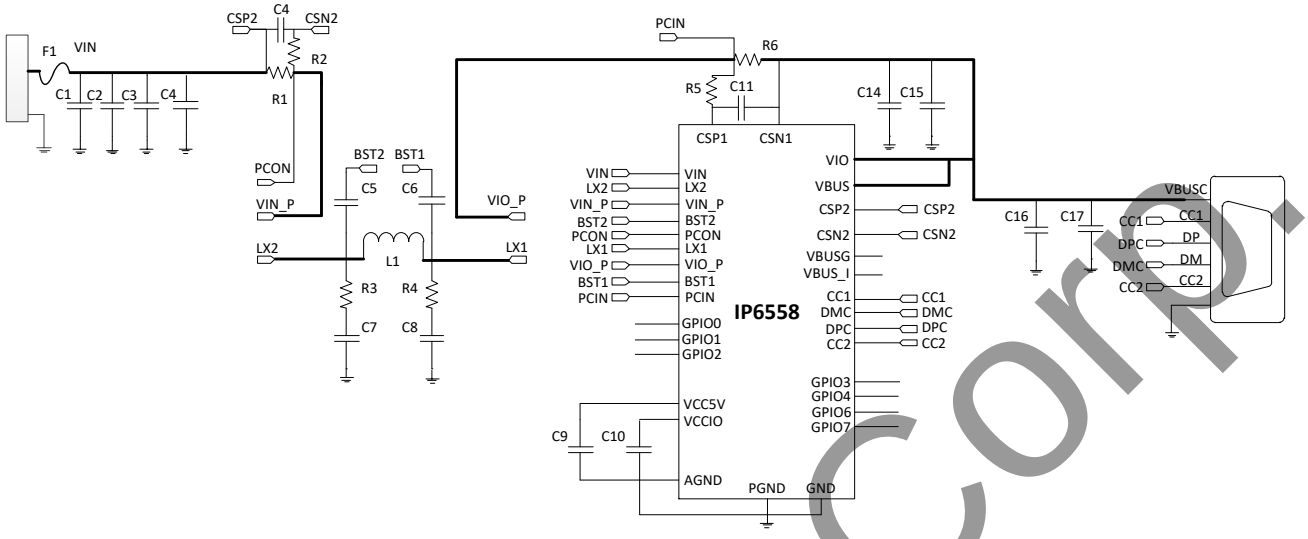


Figure 2 Simplified application schematic diagram of IP6558 single C port output

6 Pin Functions

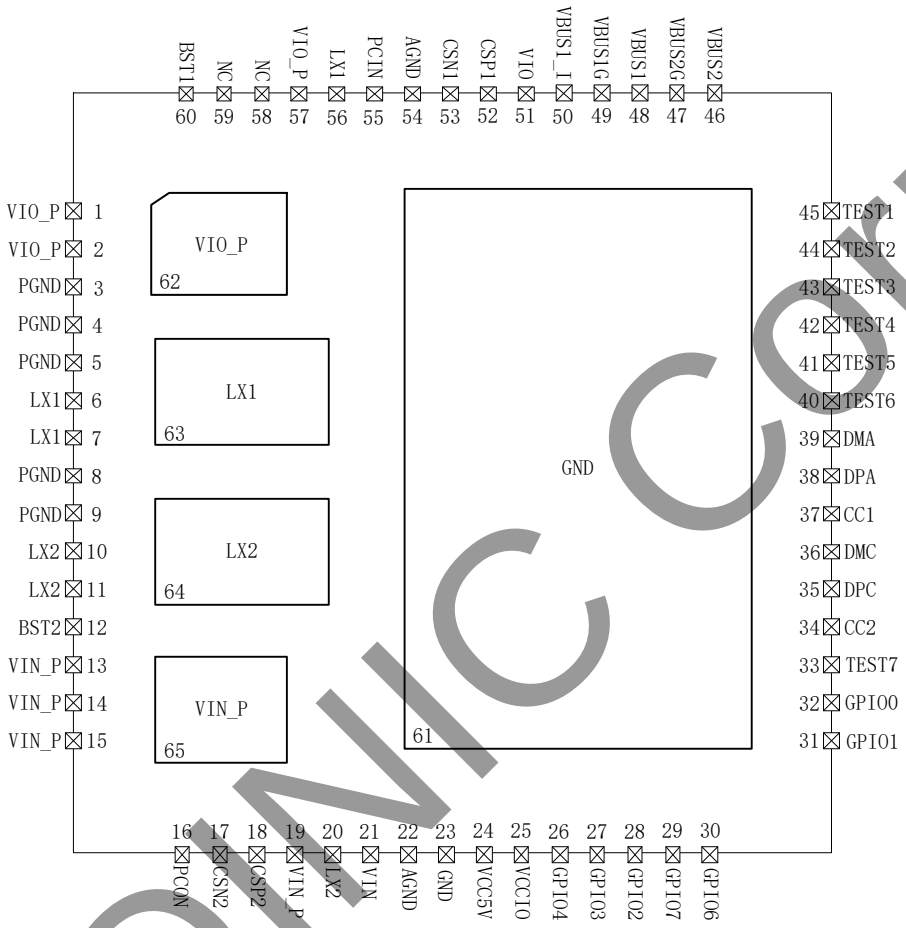


Figure 3 IP6558 Pin functions

Pin Description:

Pins		Description
Pin No.	Pin Name	
1	VIO_P	Power pin of VIO
2	VIO_P	Power pin of VIO
3	PGND	Power ground
4	PGND	Power ground
5	PGND	Power ground
6	LX1	Inductor connection pin at the VIO of the H-bridge power tube
7	LX1	Inductor connection pin at the VIO of the H-bridge power tube
8	PGND	Power ground

9	PGND	Power ground
10	LX2	Inductor connection pin at the VIN of the H-bridge power tube
11	LX2	Inductor connection pin at the VIN of the H-bridge power tube
12	BST2	Bootstrap voltage pin at the VIN of the H-bridge power tube
13	VIN_P	Power pin of VIN
14	VIN_P	Power pin of VIN
15	VIN_P	Power pin of VIN
16	PCON	Peak current sampling pin of VIN
17	CSN2	Current sampling negative terminal of VIN
18	CSP2	Current sampling positive terminal of VIN
19	VIN_P	Power pin of VIN
20	LX2	Inductor connection pin at the VIN of the H-bridge power tube
21	VIN	Supply pin of VIN
22	AGND	Analog ground
23	GND	System ground
24	VCC5V	VCC5V 5V LDO output pin
25	VCCIO	VCCIO 3.3V LDO output pin
26	GPIO4	General GPIO/Analog input
27	GPIO3	General GPIO/Analog input
28	GPIO2	General GPIO/Analog input
29	GPIO7	General GPIO/Analog input
30	GPIO6	General GPIO/Analog input
31	GPIO1	General GPIO/Analog input
32	GPIO0	General GPIO/Analog input
33	TEST7	Test pin
34	CC2	USB C port detection and fast charge communication pin CC2
35	DPC	USB C port fast charge communication pin DP
36	DMC	USB C port fast charge communication pin DM
37	CC1	USB C port detection and fast charge communication pin CC1
38	DPA	USB A port fast charge communication pin DP
39	DMA	USB A port fast charge communication pin DM
40	TEST6	Test pin
41	TEST5	Test pin
42	TEST4	Test pin
43	TEST3	Test pin
44	TEST2	Test pin
45	TEST1	Test pin

46	VBUS2	Current-sense negative input/voltage-sense pin of NMOS on VBUS1 path
47	VBUS2G	NMOS in port2 output path driver pin
48	VBUS1	Current-sense negative input/voltage-sense pin of NMOS on VBUS2 path
49	VBUS1G	NMOS in port1 output path driver pin
50	VBUS1_I	Current-sense positive input to NMOS on VBUS1 path
51	VIO	Supply pin of VIO
52	CSP1	Current sampling positive terminal of VIO
53	CSN1	Current sampling negative terminal of VIO
54	AGND	Analog ground
55	PCIN	Peak current sampling pin of VIO
56	LX1	Inductor connection pin at the VIO of the H-bridge power tube
57	VIO_P	Power pin of VIO
58	NC	Test pin, floating
59	NC	Test pin, floating
60	BST1	Bootstrap voltage pin at the VIO of the H-bridge power tube
61	GND	The system and heat dissipation ground. Must be in good contatct with GND
62	VIO_P	Power pin of VIO
63	LX1	Inductor connection pin at the VIO of the H-bridge power tube
64	LX2	Inductor connection pin at the VIN of the H-bridge power tube
65	VIN_P	Power pin of VIN

7 IP Series Model Selection Table

7.1 IC Model Selection Table

IC Model	Output current	Dual ports	Supported Protocols										Package	
			DCP	QC2.0	QC3.0	FCP	SCP	AFC	MTK PE	SFCP	PD2.0	PD3.0 (PPS)	Pkg	P2P
IP6536	2.4A	√	√	-	-	-	-	-	-	-	-	-	ESOP8	PIN2PIN
IP6523S_NU	3.4A	-	√	-	-	-	-	-	-	-	-	-	ESOP8	
IP6525TQ	18W	-	√	√	√	√	-	√	-	-	-	-	ESOP8	
IP6546	3A	√	√	-	-	-	-	-	-	-	-	-	SOP8L	PIN2PIN
IP6535	36W	-	√	√	√	√	-	√	-	-	-	-	SOP8L	
IP6525T_NU	18W	-	√	√	√	√	-	√	-	-	-	-	ESOP8	PIN2PIN
IP6525S_OC	18W	-	√	√	√	√	√	√	-	√	-	-	ESOP8	
IP6520	18W	-	√	√	√	√	√	√	√	-	√	-	ESOP8	PIN2PIN
IP6520T	20W	-	√	√	√	√	-	√	-	-	√	-	ESOP8	
IP6520T_PPS	20W	-	√	√	√	√	-	√	-	-	√	√	ESOP8	
IP6537U_C	18W	-	√	√	√	√	-	√	√	√	√	√	QFN24	
IP6529_C	27W	-	√	√	√	√	-	√	-	-	√	√	QFN24	
IP6565_CC	20W	√	√	√	√	√	-	√	-	√	√	√	QFN32	PIN2PIN
IP6565_AC	20W	√	√	√	√	√	√	√	-	√	√	√	QFN32	
IP6538U_AC	27W	√	√	√	√	√	√	√	√	-	√	√	QFN32	
IP6551	4.8A	√	√	-	-	-	-	-	-	--	-	-	QFN32	
IP6527U_C	27W	-	√	√	√	√	-	√	√	-	√	√	QFN32	
IP6559_C	100W	-	√	√	√	√	√	√	-	-	√	√	QFN64	
IP6557_C	140W	-	√	√	√	√	√	√	-	-	√	√	QFN40	PIN2PIN
IP6557_AC	140W	√	√	√	√	√	√	√	-	-	√	√	QFN40	
IP6557_CC	140W	√	√	√	√	√	√	√	-	-	√	√	QFN40	
IP6558_C	45W	-	√	√	√	√	√	√	-	-	√	√	QFNWB 60L	

7.2 IP6558 Series Product Selection

Product	Product
IP6558_C	Single C port output 45W PD fast charging output device.
IP6558_AC	USBA and USBC dual port output with path NMOS control, either port supports fast charge output.

Notes：

1、IP6558_AC shares power 5V4.8A on both ports when both ports are plugged in at the same time.

8 Internal Block Diagram

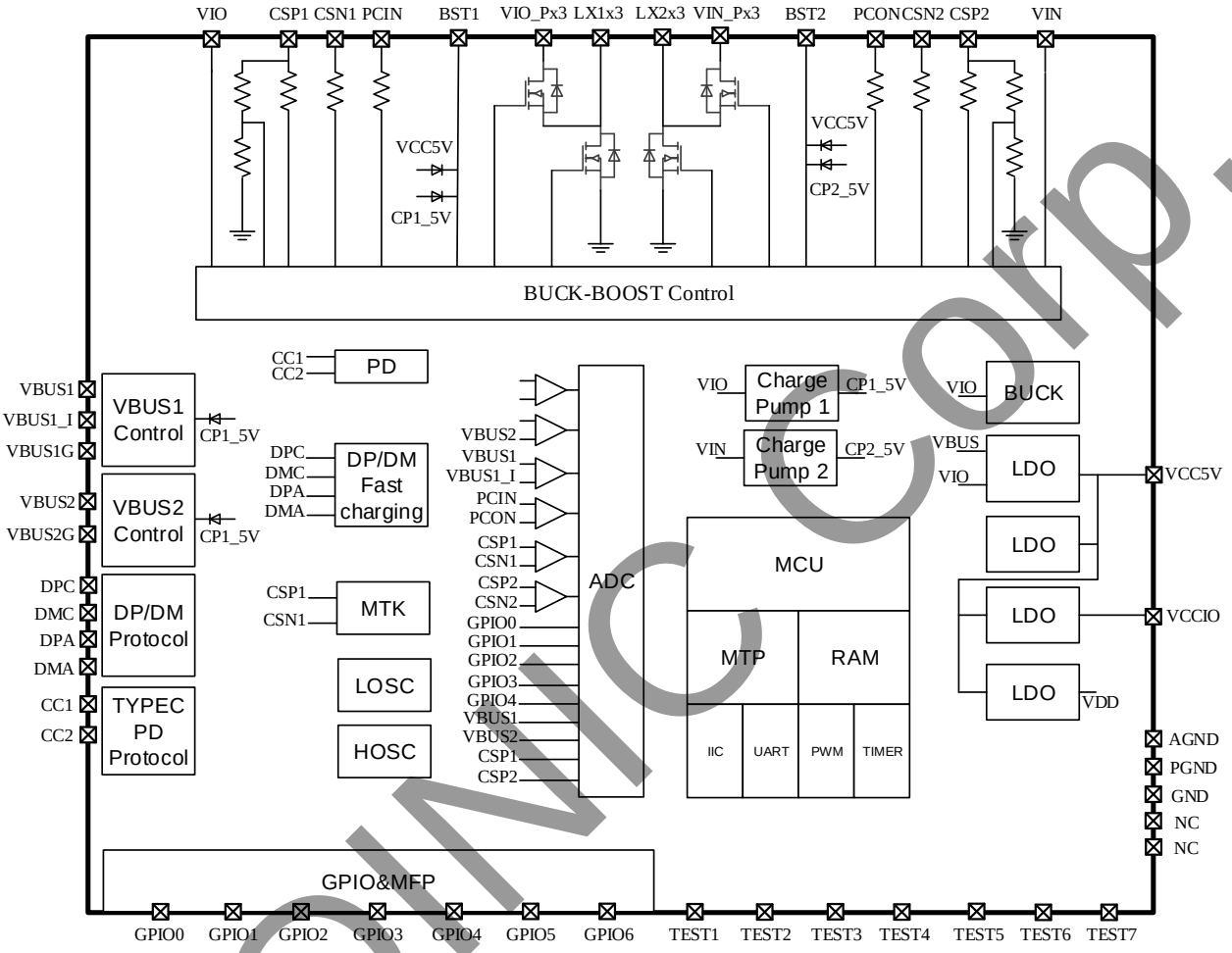


Figure 4 IC Internal block diagram

9 Absolute Maximum Ratings

Parameters	Symbol	Value	Unit
Input voltage	V_{IN}	-0.3 ~ 32	V
VBUS1/VBUS2 voltage	$V_{VBUS1/VBUS2}$	-0.3 ~ 30	V
VIO voltage	V_{VIO}	-0.3 ~ 30	V
LX1/BST1/LX2/BST2 voltage	$V_{LX1/BST1/LX2/BST2}$	（-3V for 10ns）-0.3 ~ 50	V
CSP2/CSN2/PCIN voltage	$V_{CSP2/CSN2/PCIN}$	-0.3 ~ 32	V
CSP1/CSN1/PCON voltage	$V_{CSP1/CSN1/PCON}$	-0.3 ~ 30	V
CC1/CC2 voltage	$V_{CC1/CC2}$	-0.3 ~ 30	V
DMC/DPC/DPA/DMA voltage	$V_{DMC/DPC/DMA/DPA}$	-0.3 ~ 22	V
GPIO voltage	$V_{GPIO1/GPIO2/GPIO3}$ $V_{GPIO4/GPIO5/GPIO6}$	-0.3 ~ 8	V
Junction temperature	T_J	-40 ~ 150	℃
Storage temperature	Tstg	-60 ~ 150	℃
Thermal resistance (junction to ambient)	θ_{JA}	45	℃/W
Human body model (HBM)	ESD	4	KV

*Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device.

Exposure to Absolute Maximum Rated conditions for extended periods may affect device reliability.

10 Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input voltage	V_{IN}	5	12/24	30	V
Working Temperature	T_A	-20		105	℃

* Device's performance cannot be guaranteed when working beyond those Recommended Operating Conditions.

11 Electrical Characteristics

Unless otherwise specified, the tested IC is IP6558_C, L=10uH, Cout=100uF, solid state Capacitor

Parameters	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Input system						
Input voltage	V_{IN}		5	12/24	30	V
Input under voltage	V_{IN-UV}	Lowering voltage	4.3	4.5	4.7	V
	$V_{IN-UV-TH}$	Hysteresis voltage		0.5		V
Input over voltage	V_{IN-OV}	Rising voltage	29.6	30	30.4	V
	$V_{IN-OV-TH}$	Hysteresis voltage		0.4		V
Input quiescent current	I_{Q1}	VIN=24V，VOUT=5V@0A		3.15		mA
Drive system						
Built-in H-bridge power Nmos on-resistance	$R_{DS（ON）}$	V_{GS}=4.5V，I_D=10A		11	13.5	mΩ
Dead time	$T_{DEADTIME}$	VIN=24V，VOUT=5V		45		ns
Switching frequency	F_S	VIN=24V，VOUT=5V	225	250	275	kHz
Output system						
Output voltage	V_{OUT}		3.3		21	V
Output Voltage Ripple	ΔV_{OUT}	VIN=24V, VOUT=5.0V, Fs=250KHz, IOUT=3A		70		mV
		VIN=24V, VOUT=12V, Fs=250KHz, IOUT=3A		90		mV
Soft start time	T_{SS}	VIN=24V，VOUT=5V	1.5	1.6	2.5	ms
Output line compensate voltage	V_{COMP}	VIN=24V ， VOUT=5V ， IOUT=3A		150		mV
Maximum Output current in CC mode	I_{OUT}	VIN=24V，VOUT=5V		3		A
		VIN=24V，VOUT=12V		3		A
		VIN=24V，VOUT=20V		2.25		A
Output overvoltage threshold	V_{OUT}	After the output enters CC mode, the output hiccup restart voltage		2.8		V
Thermal shutdown temperature	T_{OTP}	Rising temperature		150		℃
Thermal shutdown temperature hysteresis	ΔT_{OTP}	Lowering temperature		40		℃

12 Function Description

12.1 Synchronized Switch Buck-Boost Converter

IP6558 integrates a Synchronous-Rectified Buck-Boost Converter, wide input voltage ranges from 5V to 30V and output from 3.3V to 21V.

IP6558 integrates input peak inductance current limiting and output average current limiting functions.

The output switching frequency of IP6558 is 250kHz, and can be adjusted internally.

IP6558 has soft start function, preventing the huge inrush current cause damage to the IC. When VIN=12V, VOUT=5V, the soft start time is 1.6ms.

Tested on demo board, VIN=12V, VOUT=5V@3A, conversion efficiency is 93%.

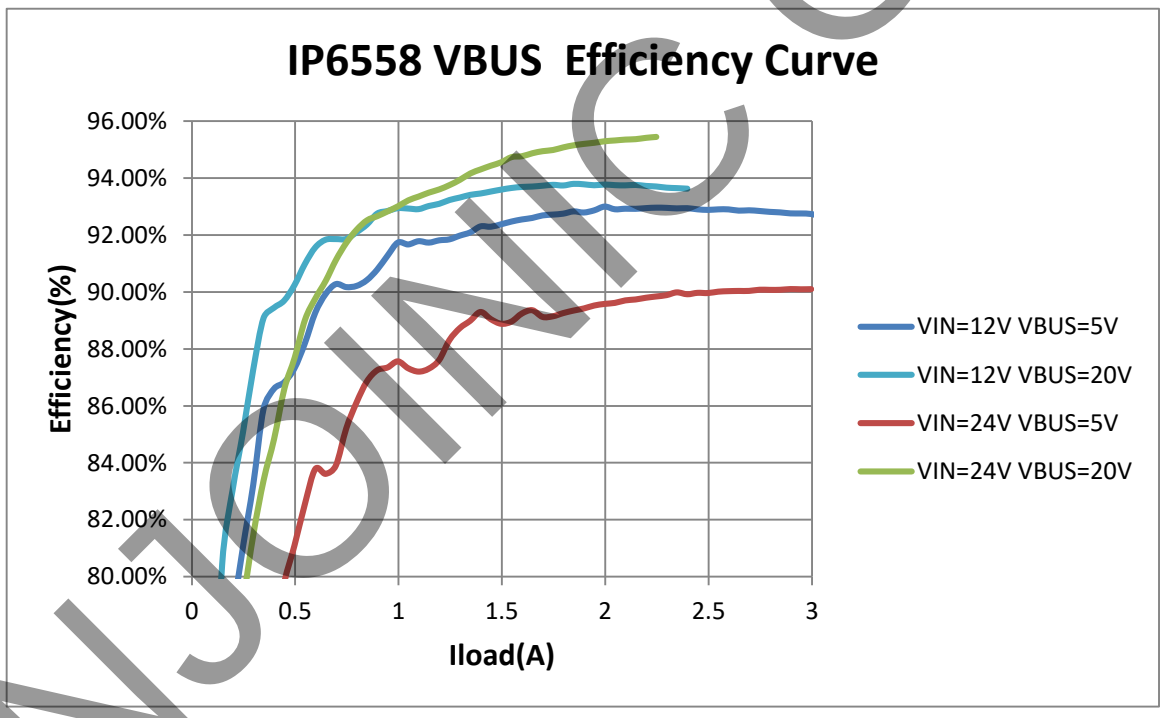


Figure 5 IP6558 VBUS output efficiency curve

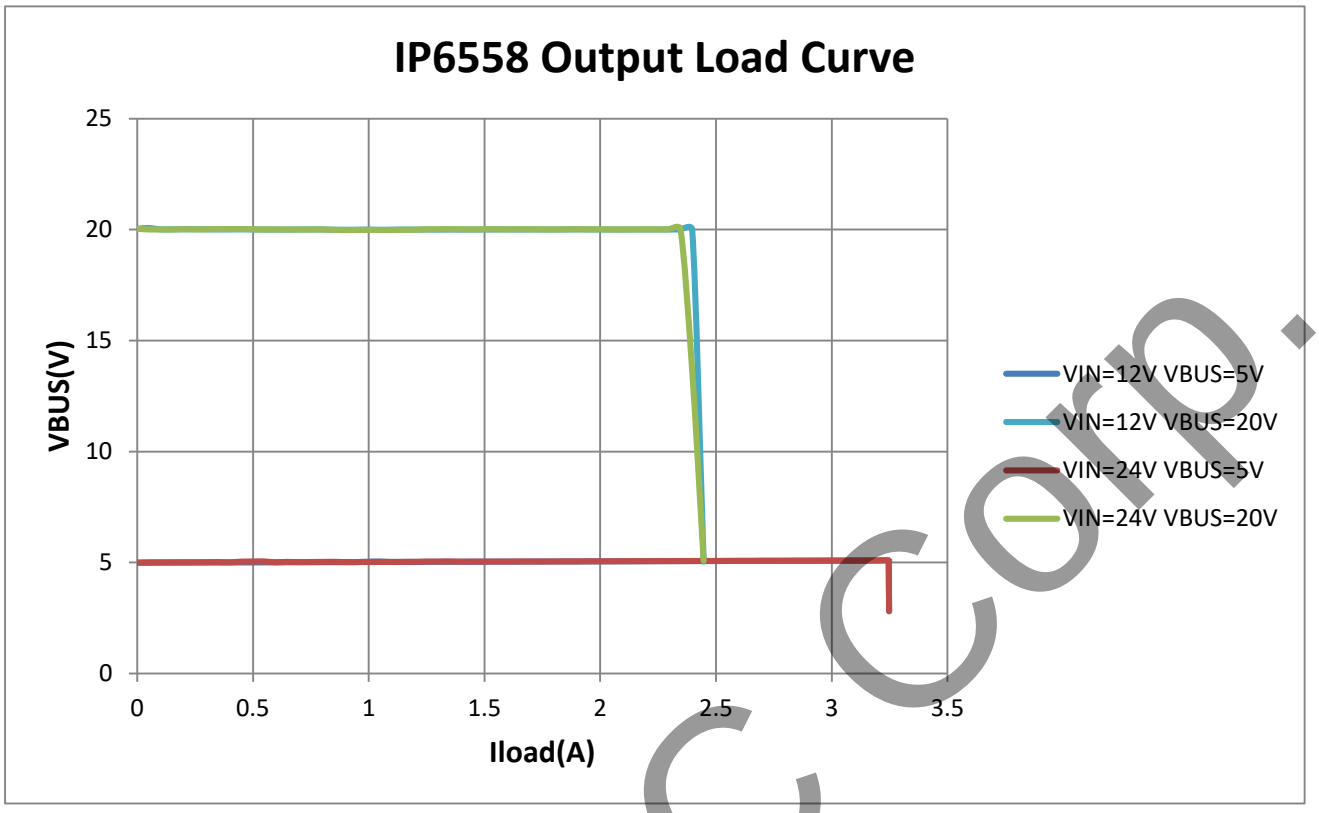


Figure 6 IP6558 VBUS output load curve

12.2 Output Voltage Line Compensate

The IP6558 has a line complement of output voltage: for every 1A increase in output current, the output voltage is increased by 50mV.

12.3 Output CV/CC Characteristic

IP6558 output has CV/CC mode: when the output current is lower than preset value, the output is in CV mode with constant voltage; when the output current is higher than preset value, the output is in CC mode with decreasing output voltage. The output current continues to increase and the output voltage rapidly decreases until the output voltage undervoltage protection is triggered.

12.4 Output CC Current Set

IP6558 can adjust the output CC current by adjusting the 5mohm current sensing resistor between CSP1 and CSN1 on the output path as shown below. By detecting the voltage difference between CSP1 and CSN1, it can determine whether the current load current is up to the set current size.

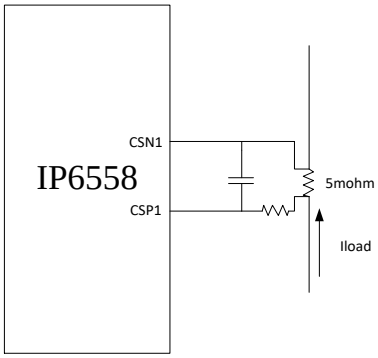


Figure 7 IP6558 output current limiting circuit

When the value of 5mohm current sensing resistor is changed, the IP6558 output current limit will be changed accordingly.

In PCB layout, pay attention to the trace routing of CSP1 and CSN1, the trace should go out directly from the two side of 5mohm resistor, avoiding introduce current limit deviation because of additional PCB trace resistor.

Other than that, the 5mohm resistor should use alloy resistor with good temperature coefficient (100ppm) and high precision of 1%.

12.5 Protection Function

IP6558 supports input over voltage protection: When the VIN voltage is higher than 30V, IP6558 will shut down the output because of the VIN over voltage. When the VIN drops under 29V, IP6558 will consider the VIN normal and reopen the output.

IP6558 supports output under voltage protection: When the VBUS voltage is lower than 2.8V, IP6558 will shut down the output because of the output under voltage. After 2sec, it will hiccup reopen.

IP6558 supports short circuit protection: 10ms after the circuit is working, when VBUS voltage is under 2.8V, IP6558 will shut down the output because of the output short circuit. After 2sec, it will hiccup reopen.

IP6558 supports over temperature protection: When the temperature is detected higher than 150℃, the output will be shut down. When the temperature drops under 110℃, IP6558 will consider the temperature normal and will reopen the output.

12.6 Fast Charge Protocol Output

IP6558 supports fast charge protocol output, the specifications are as follows:

- ✧ Support BC1.2 and Apple protocol
- ✧ Support PD2.0/PD3.1/PPS protocol
- ✧ Support QC2.0/QC3.0/QC3.0+/ QC4+/QC5 protocol
- ✧ Support FCP/HSCP protocol
- ✧ Support AFC protocol
- ✧ Support MTK protocol
- ✧ Support UFCS protocol

13 Application Notes

13.1 Input Capacitance Selection

The ESR of the input capacitor should be as small as possible. The ESR will affect the conversion efficiency of the system.

When the input voltage is significantly greater than the output voltage, the device works in buck mode. The maximum ripple current supported by the input capacitor must be greater than the maximum VIN ripple current of the system. The ripple current RMS value ($I_{RMS(VIN)}$) of the input capacitor is calculated as follows:

$$I_{RMS(VIN)} = I_{LOAD} * \sqrt{\frac{V_{OUT}}{V_{IN}} * (1 - \frac{V_{OUT}}{V_{IN}})}$$

I_{LOAD} is the output current, V_{IN} is the input voltage, V_{OUT} is the output voltage.

13.2 Inductance Selection

The inductor with 4.7uH is recommended for most applications.

The DCR of inductor has great influence on the conversion efficiency of the system, low DCR inductors are recommended. For solutions above 30W, it is recommended to use an inductor with a DCR of less than 10mohm.

The inductor saturation current should be at least 20% greater than the system's peak inductor current limit, in order to avoid inductance saturation, resulting in a decrease in inductance, system instability.

The calculation formula of the PEAK current ($I_{L(PEAK)-BUCK}$) in buck mode is as follows:

$$I_{L(PEAK)-BUCK} = I_{LOAD} + \frac{V_{OUT}*(V_{IN}-V_{OUT})}{2*V_{IN}*F_S*L}$$

The calculation formula of the PEAK current ($I_{L(PEAK)-BOOST}$) in boost mode is as follows:

$$I_{L(PEAK)-BOOST} = \frac{V_{OUT}*I_{LOAD}}{V_{IN}*EFF} + \frac{V_{IN}*(V_{OUT}-V_{IN})}{2*V_{OUT}*F_S*L}$$

I_{LOAD} is the output current, V_{IN} is the input voltage, V_{OUT} is the output voltage, L is the inductance, F_S is the switching frequency，EFF is the conversion efficiency of DCDC.

13.3 Output Capacitance Selection

When the output voltage is significantly greater than the input voltage, the device works in boost mode. The maximum ripple current supported by the output capacitor must be greater than the maximum VOUT ripple current of the system. The ripple current RMS value ($I_{RMS(VOUT)}$) of the output capacitor is calculated as follows:

$$I_{RMS(VOUT)} = I_{LOAD} * \sqrt{(\frac{V_{OUT}}{V_{IN}} - 1)}$$

I_{LOAD} is the output current, V_{IN} is the input voltage, V_{OUT} is the output voltage.

The output capacitance is used to keep the output stable. The value of ESR and capacitance has an effect on the output ripple.

The output ripple voltage $V_{OUT(RIPPLE)-BUCK}$ in buck mode can be calculated as follows：

$$V_{OUT(RIPPLE)-BUCK} = \frac{V_{OUT}*(V_{IN}-V_{OUT})}{V_{IN}*L*F_S} * (R_{ESR} + \frac{1}{8*F_S*C_{OUT}})$$

R_{ESR} is the equivalent serial resistance value of the output capacitance, F_S is the switching frequency, C_{OUT} is the output capacitance value.

The output ripple voltage $V_{OUT(RIPPLE)-BOOST}$ in boost mode can be calculated as follows:

$$V_{OUT(RIPPLE)-BOOST} = \frac{I_{LOAD}*V_{OUT}*R_{ESR}}{V_{IN}} + \frac{(V_{OUT}-V_{IN})*I_{LOAD}}{V_{OUT}*F_S*C_{OUT}}$$

R_{ESR} is the equivalent serial resistance value of the output capacitance, F_S is the switching frequency, C_{OUT} is the output capacitance value.

14 Typical Application Schematic

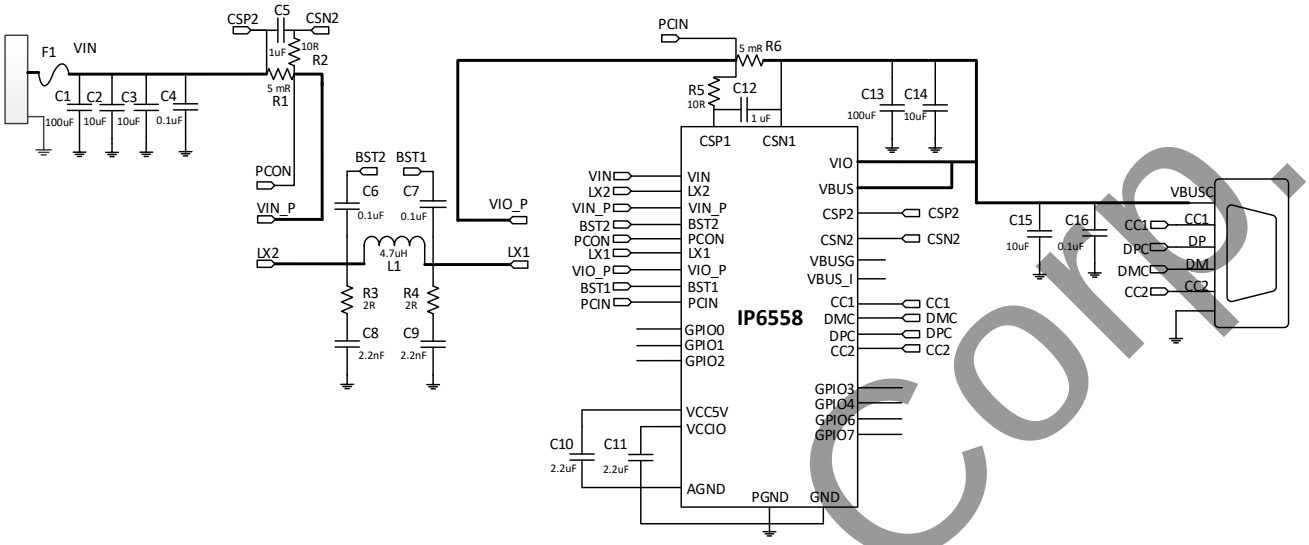


Figure 8 Typical application schematic diagram of IP6558 single C port

15 BOM

With the application of IP6558 single USBC output port, the finished BOM is as follows:：

No.	Part Name	Type	Location	Qty	Notes
1	IC	IP6558_C	U1	1	
2	SMD capacitor	0603 100nF 10% 50V	C6,C7	2	
3	SMD capacitor	0603 100nF 10% 35V	C4 ,C16	2	
4	SMD capacitor	0603 1μF 10% 35V	C5,C12	3	
5	SMD capacitor	0603 2.2μF 10% 16V	C10,C11	2	
6	SMD capacitor	0603 2.2nF 10% 50V	C8,C9	4	
7	SMD capacitor	0805 10μF 10% 35V	C2,C3,C14,C15	4	
8	Solid-state capacitor	100μF 35V 10%	C1,C13	2	
9	SMD resistor	1206 0.005R 1%	R1,R6	2	Sampling resistor, requires the use of high-precision low-temperature drift metal film resistors
10	SMD resistor	0603 2R 5%	R3,R4	2	
11	SMD resistor	0603 10R 5%	R2,R5	2	
12	Inductor	4.7μH 9A R_{DC}<10mR	L1	1	
13	Fuse	Fuse	F1	1	

16 Precautions for PCB layout

IP6558 integrates a Synchronous-Rectified Buck-Boost converter. PCB layout is important for system stability, EMI, and other performance indicators. The PCB layout suggestions are as follows:

1. The loop formed by the input capacitor and the H-bridge power down tube VIN_P is as small as possible.

2. The loop formed by the output capacitor and the H-bridge power down tube VIO_P is as small as possible.

3. The LX1/LX2 inductor alignment is as wide as possible, and the area of the node is sufficient to ensure maximum output current capability.

4. The loop composed of LX1/LX2 buffer circuit and PGND should be as small as possible.

5. Pin VIN, CSP2 belongs to the same network, but the alignment must be separate from the 5mohm sampling resistor side of the lead, CSN2 and PCON also need to be separate from the other side of the 5mohm sampling resistor lead, VIO and VIN side of the sampling resistor alignment is the same; which the sampling line of the RC (R2/C5/R5/C12) need to be placed close to the chip pins, the sampling line needs to be parallel alignment, as short as possible and avoid open joints such as LX/BST.

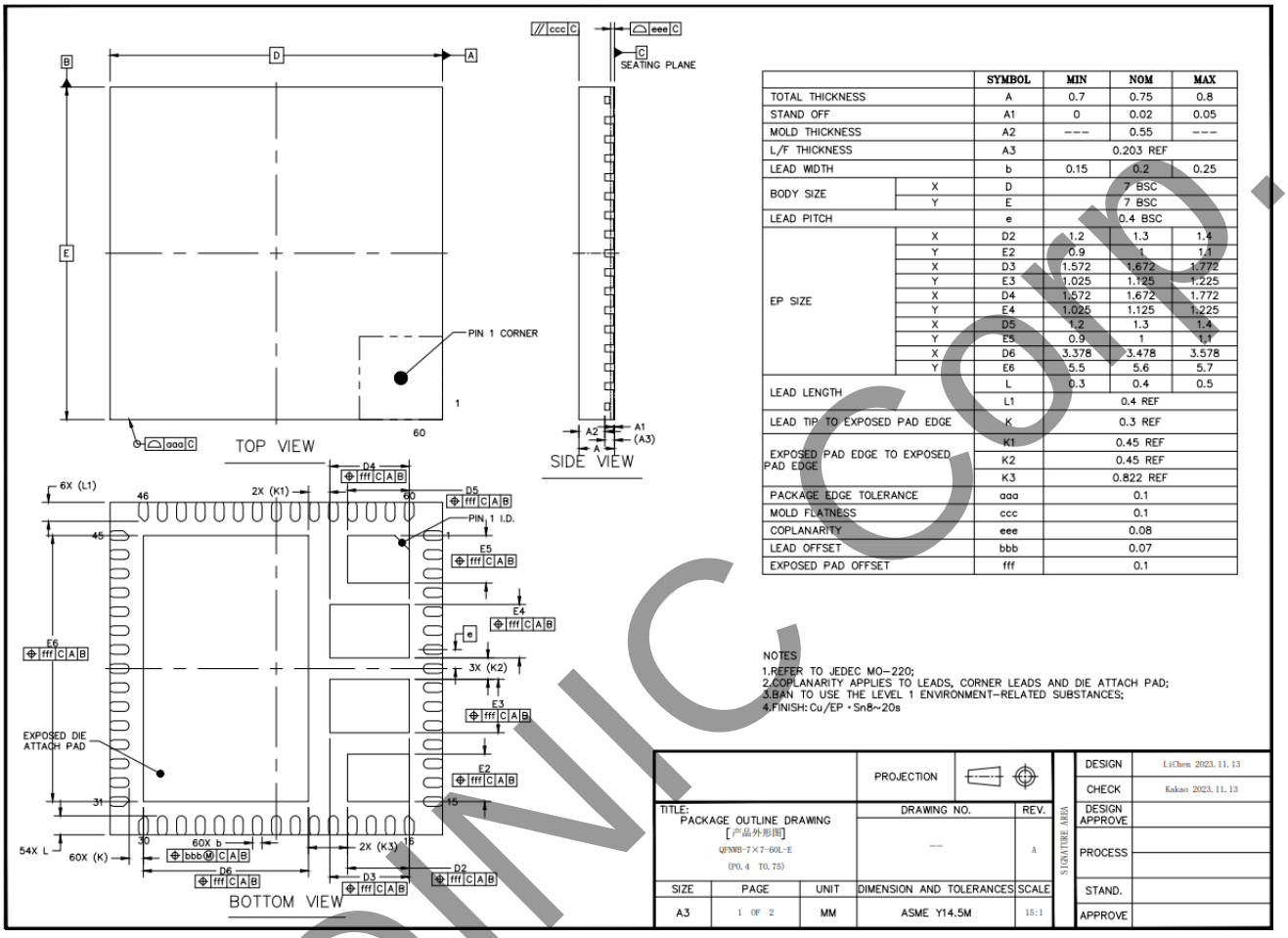
6. The capacitors of VCC5V and VCCIO is placed close to the chip pins.

7. The GND of the input and output capacitors must be connected to the PGND of a large area.

8. For better ESD protection, it is recommended to reserve the positions of resistors in series and diodes to ground in the CC1/CC2/DP/DM lines, and reserve capacitors to ground in CC1/CC2.

9. At least one 10uF capacitor is placed next to the 5mohm sampling resistor of VIO_P and VIN, and the GND of the capacitor must be close to the PGND of the H-bridge power downtube, and more over-holes are needed between the GND of the capacitor and the PGND of the H-bridge power downtube. Otherwise the current sampling and system stability may be affected.

17 Package



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.55	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.15	0.2	0.25
BODY SIZE	X	D		7 BSC	
	Y	E		7 BSC	
LEAD PITCH		e		0.4 BSC	
EP SIZE	X	D2	1.2	1.3	1.4
	Y	E2	0.9	1	1.1
	X	D3	1.572	1.672	1.772
	Y	E3	1.025	1.125	1.225
	X	D4	1.572	1.672	1.772
	Y	E4	1.025	1.125	1.225
	X	D5	1.2	1.3	1.4
	Y	E5	0.9	1	1.1
	X	D6	3.378	3.478	3.578
	Y	E6	5.5	5.6	5.7
LEAD LENGTH		L	0.3	0.4	0.5
		L1		0.4 REF	
LEAD TIP TO EXPOSED PAD EDGE		K		0.3 REF	
EXPOSED PAD EDGE TO EXPOSED PAD EDGE		K1		0.45 REF	
		K2		0.45 REF	
		K3		0.822 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.08	
LEAD OFFSET		bbb		0.07	
EXPOSED PAD OFFSET		fff		0.1	

NOTES
1.REFER TO JEDEC MO-220;
2.COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD;
3.BAN TO USE THE LEVEL 1 ENVIRONMENT-RELATED SUBSTANCES;
4.FINISH: Cu/EP · Sn8~20s

PROJECTION			DESIGN	LiChen 2023.11.13
TITLE: PACKAGE OUTLINE DRAWING [产品外形图] QFNWB-7×7-60L-E (P0.4 T0.75)	DRAWING NO. ---	REV. A	CHECK	Kakao 2023.11.13
			DESIGN APPROVE	
			PROCESS	
SIZE A3	PAGE 1 OF 2	UNIT MM	DIMENSION AND TOLERANCES ASME Y14.5M	SCALE 15:1
			STAND.	
			APPROVE	

SIGNATURE AREA

Figure 9 Package diagram

18 Silkscreen Description

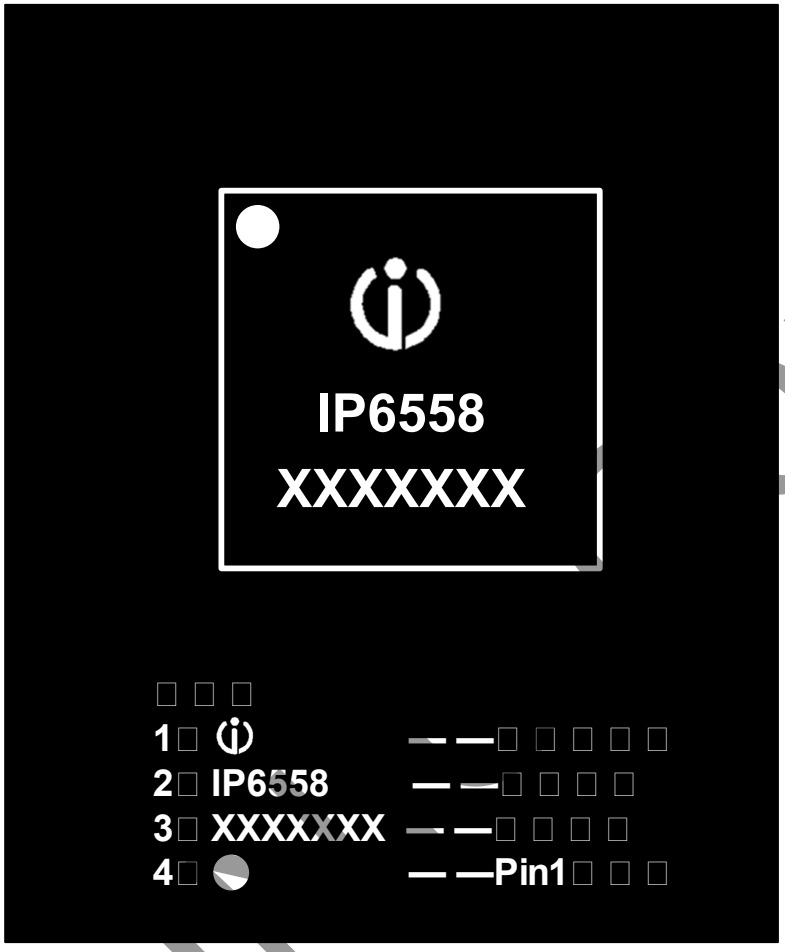


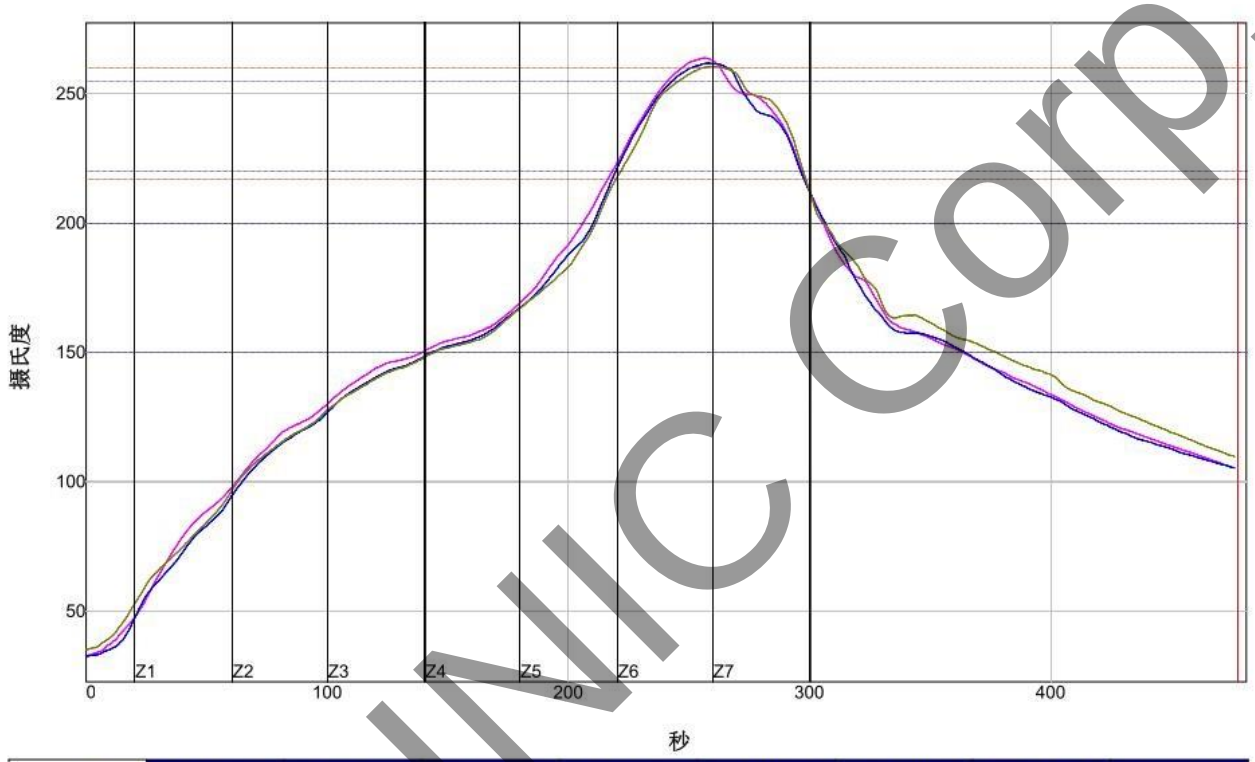
Figure 10 Silkscreen diagram

19 Soldering Temperature

温度设置 (摄氏度)

温区	1	2	3	4	5	6	7
上温区	130	140	160	160	200	230	265
下温区	130	140	160	160	200	230	265

传送带速度 (公分/分): 39.0



PWI= 75%	最高上升斜率		预热150至200C		最高温度		总共 时间 /217C		斜率1 (217-260C)		预热220至255C-(2)		总共 时间 /260C-2		距峰值5C区域时间	
VP 1	1.69	-31%	66.21	-59%	263.87	18%	80.99	-70%	1.70	-30%	22.81	-36%	15.90	-30%	18.13	-75%
VP 2	1.99	-1%	66.91	-54%	261.84	-9%	78.97	-73%	1.87	-13%	23.44	-33%	15.74	-31%	23.64	-31%
VP 3	1.83	-17%	66.61	-56%	260.76	-23%	78.19	-74%	1.88	-12%	23.97	-30%	9.37	-66%	23.95	-28%
温差	0.30		0.70		3.11		2.80		0.18		1.16		6.53		5.82	

制程界限:

锡膏: 260

统计数名称	最低界限	最高界限	单位
最高温度上升斜率 (目标=2.0) (计算斜率的时间距离= 20 秒)	1.0	3.0	度/秒
斜率1 (目标=2.0) 介于 217.0 和 260.0 (计算斜率的时间距离= 10 秒)	1.0	3.0	度/秒
预热时间150-200摄氏度	60	90	秒
预热时间220-255摄氏度-(2)	10	50	秒
最高温度	255	270	度 摄氏度
在217摄氏度以上时间	60	200	秒
在260摄氏度以上时间-(2)	3	40	秒
距峰值5C区域时间	15	40	秒

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