Buck-Boost SOC with Type-C PD3.0 (PPS) Protocol

1 Features

- **Synchronous-rectified Buck-Boost converter**
  - ✧ Input voltage range: 3.6V~31V
  - ✧ Support gate driver of path NMOS
  - ✧ Support line compensate function
  - ✧ Support CV/CC output mode
- **Type-C and PD protocol**
  - ✧ Support 5V/9V/12V/15V/20V output
  - ✧ Support PD2.0/PD3.0(PPS) protocol
  - ✧ Support 3.3V-21V, 20mV/step PPS
  - ✧ Support E-MARK cable
- **Fast charge output**
  - ✧ Support Type-C and PD protocol
  - ✧ Support BC1.2 and Apple protocol
  - ✧ Support QC2.0/ QC3.0/ QC3+ protocol
  - ✧ Support FCP/SCP protocol
  - ✧ Support AFC protocol
  - ✧ Support VOOC protocol
- **Dual output ports**
  - ✧ Dual ports automatic detection of device plug-in and plug-out
  - ✧ Support AC output
- **Voltage and current acquisition and display**
  - ✧ Built-in 14-bit ADC
  - ✧ Input and output voltage and current acquisition and display
- **Multi-protection and high reliability**
  - ✧ Support input OVP and UVP
  - ✧ Support output OVP, OCP and SCP
  - ✧ Over temperature protection
  - ✧ NTC Board-level temperature detection
  - ✧ ESD 4KV

2 Applications

- **Car Charger**
- **Fast Charge Adaptor**

3 Description

IP6559 integrates a Synchronous-Rectified Buck-Boost driver and Type-C and PD fast charge protocol. It provides solutions for car charger, fast charge adaptor.

IP6559 supports up to 31V input voltage, integrated input and output current limiting functions.

IP6559 supports NTC board-level temperature detection, can intelligently adjust the output power according to the temperature.

IP6559 integrates built-in 14-bit ADC to accurately measure the voltage and current of the input and output, and supports display function.

IP6559 supports output line compensation function to get stable output voltage.

IP6559 supports soft start function that protects the input power source from inrush current at start up.

IP6559 supports multi-protection on input overvoltage and under voltage, output over current, overvoltage, under voltage and short circuit protection.

Package: QFN48(7*7)

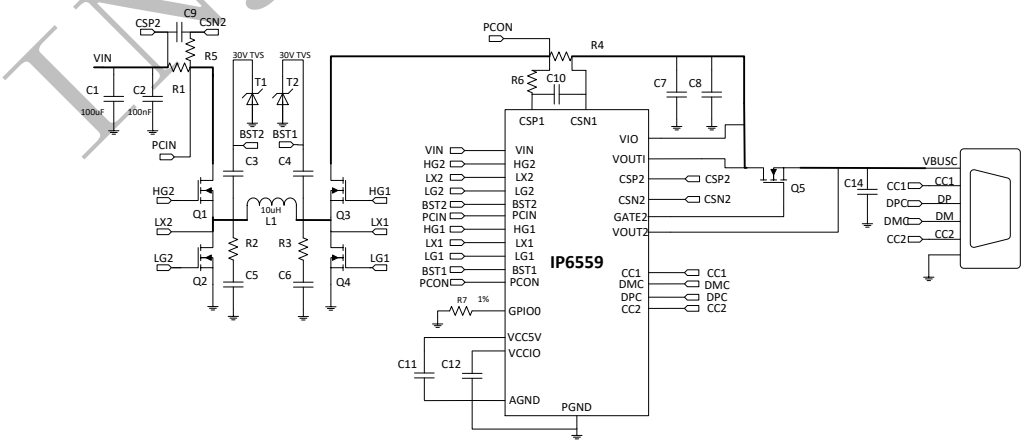


Figure 1. Simplified application schematic diagram of IP6559 single C port with digital tube display output

4 Pin Functions

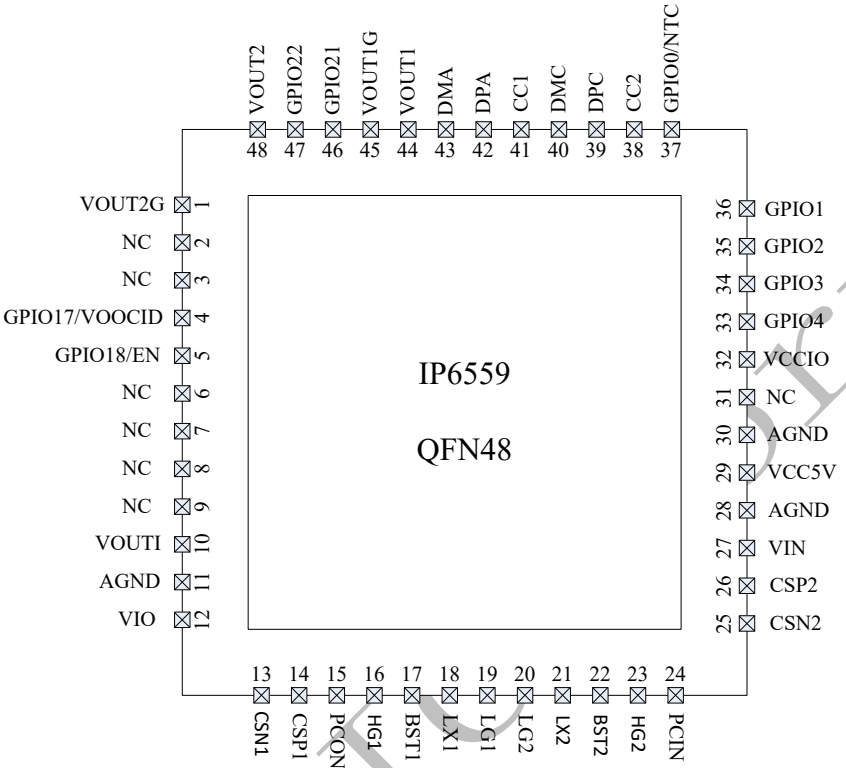


Figure 2. Pin functions

Pins		Description
Pin No.	Pin Name	
1	VOUT2G	NMOS in port1 output path driver pin
2	NC	Test pin, floating
3	NC	Test pin, floating
4	GPIO17/VOOCID	General GPIO/VOOC ID identification pin
5	GPIO18/EN	General GPIO/EN pin
6	NC	Test pin, floating
7	NC	Test pin, floating
8	NC	Test pin, floating
9	NC	Test pin, floating
10	VOUTI	Path MOS current detection positive input
11	AGND	Analog ground
12	VIO	Buck-boost output voltage feedback pin
13	CSN1	Current sampling negative terminal of VIO
14	CSP1	Current sampling positive terminal of VIO
15	PCON	Output peak current sampling pin
16	HG1	The upper tube control pin at H-bridge power output end
17	BST1	Bootstrap voltage pin at the output of the H-bridge power tube
18	LX1	Inductor connection pin at the output of the H-bridge power tube

19	LG1	The lower tube control pin at H-bridge power output end
20	LG2	The lower tube control pin at H-bridge power input end
21	LX2	Inductor connection pin at the input of the H-bridge power tube
22	BST2	Bootstrap voltage pin at the input of the H-bridge power tube
23	HG2	The upper tube control pin at H-bridge power input end
24	PCIN	Input peak current sampling pin
25	CSN2	Current sampling negative terminal of VIN
26	CSP2	Current sampling positive terminal of VIN
27	VIN	VIN input pin
28	AGND	Analog ground
29	VCC5V	VCC5V 5V LDO output pin
30	AGND	Analog GND
31	NC	Test pin, floating
32	VCCIO	VCCIO 3.3V LDO output pin
33	GPIO4	General GPIO/Analog input
34	GPIO3	General GPIO/ Analog input
35	GPIO2	General GPIO/ Analog input
36	GPIO1	General GPIO/ Analog input
37	GPIO0/NTC	General GPIO/ Analog input/NTC resistance detection pin
38	CC2	USB C port detection and fast charge communication pin CC2
39	DPC	USB C port fast charge communication pin DPC
40	DMC	USB C port fast charge communication pin DMC
41	CC1	USB C port detection and fast charge communication pin CC1
42	DPA	USB A port fast charge communication pin DPA
43	DMA	USB A port fast charge communication pin DMA
44	VOUT1	Port1 output path MOS current detection negative input
45	VOUT1G	NMOS in port1 output path driver pin
46	GPIO21	General GPIO
47	GPIO22	General GPIO
48	VOUT2	Port2 output path MOS current detection negative input
49	EPAD	Power GND

5 IP6559 Series Product Introduction

Product	Introduction
IP6559	Single C port 65W output; IP6559+IP6525S_OC/ IP6525S_PS_24W support USBA and USBC dual output ports with intelligent power reduction function;
IP6559_AC	USBA and USBC dual port output, either port supports fast charge output;
IP6559_C	Single C port 100W PD fast charge output, supports path NMOS control function;

Notes:

1. In Figure 8 and Figure 9, adjusting the resistance R7 can change the PDO of IP6559_C port C;

2. In Figure 10, adjusting the resistance R7 can change the PDO of IP6559_C port C, and adjusting the resistance R8 can Change the output power of IP6559_C port A;

3. IP6559_AC can be used with other ICs for power sharing. After the CC of IP6559_AC is successfully connected, GPIO17 will output a high level; if GPIO18 detects a high level, port C will reduce the power. When IP6559_AC is used alone, GPIO18 needs to be grounded to prevent interference;

4. In Figure 11, adjusting the ground resistance R10/R11/R12 can change the PDO of IP6559 port C in different states of the dual ports; If you don't want to reduce power in corresponding state, the R11 or R12 is not need;

5. For the correspondence between resistance value and PDO, please refer to the IP6559 application description document;

6. In the intelligent power reduction function, if you choose the USBA port priority mode, you need to choose the IP6525S_OC; or you choose the USBC port priority mode, you need to choose the IP6525S_PS_24W; please refer to the IP6559 application description document;

6 Absolute Maximum Ratings

Parameters	Symbol	Value	Unit
Input voltage	V_{IN}	-0.3 ~ 34	**V**
LX voltage	V_{LX}	-0.3 ~ VIN+0.3	**V**
BST voltage	V_{BST}	-0.3 ~ 42	**V**
VOUT1/VOUT2 voltage	$V_{VOUT1/VOUT2}$	-0.3 ~ 25	**V**
DM/DP voltage	$V_{DM/DP}$	-0.3 ~ 6	**V**
Junction temperature	T_J	-40 ~ 150	℃
Storage temperature	Tstg	-60 ~ 150	℃
Thermal resistance (junction to ambient)	θ_{JA}	30	**℃/W**
Human body model (HBM)	ESD	4	**KV**

*Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to Absolute Maximum Rated conditions for extended periods may affect device reliability.

7 Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input voltage	V_{IN}	3.6		31	V

*Device's performance cannot be guaranteed when working beyond those Recommended Operating Conditions.

8 Electrical Characteristics

Unless otherwise specified, the test IC is IP6559_C, TA =25℃, L=10uH, VIN=12V, VOUT2=5V

Parameters	Symbol	Test Condition	Min.	Typ.	Max	Unit
Input system						
Input voltage	V_{IN}		3.6		31	V
Input under voltage	V_{IN-UV}	Rising voltage	3.2	3.6	3.7	V
	$V_{IN-UV-TH}$	Hysteresis voltage		0.2		V
Input over voltage	V_{IN-OV}	Rising voltage	30.5	31	32	V
	$V_{IN-OV-TH}$	Hysteresis voltage		2		V
Input quiescent current	I_Q	VIN=12V, VOUT2=5V@0A, no switching		10		mA
Shutdown current	I_{SD}	VIN=12V，EN=0V		200		uA
Drive system						
HG1/HG2 pull-up resistor	R_{HG_PU}			2		Ω
HG1/HG2 pull-down resistor	R_{HG_PD}			1		Ω
LG1/LG2 pull-up resistor	R_{LG_PU}			2		Ω
LG1/LG2 pull-down resistor	R_{LG_PD}			1		Ω
Dead time	T_{Dead}	VIN=12V，VOUT2=5V		50		ns
Switching frequency	F_S	VIN=12V，VOUT2=5V		250		kHz
Output system						
Output voltage	V_{OUT}		3		20	V
Output voltage ripple Cout: 100uf solid-state cap	ΔV_{OUT}	VIN=12V，VOUT2=5V@3A	30	40	60	mV
		VIN=12V，VOUT2=20V@5A	70	80	90	
Soft start time	T_{SS}	VIN=12V，VOUT2=5V		4.75		ms
Output line compensate voltage	V_{COMP}	VIN=12V，VOUT2=5V，IOUT=1A		30		mV
Output current in CC mode	I_{OUT}	VIN=12V，VOUT2=5V		3		A
		VIN=12V，VOUT2=9V		3		A
		VIN=12V，VOUT2=12V		3		A
		VIN=12V，VOUT2=20V E-MARK cable		5		A
Output overvoltage threshold	V_{OUT}	After the output enters CC		2.6		V

		mode, the output hiccup restart voltage				
Thermal shutdown temperature	T_{OTP}	Rising temperature		150		℃
Thermal shutdown temperature hysteresis	ΔT_{OTP}			40		℃

9 Function Description

Internal Block Diagram

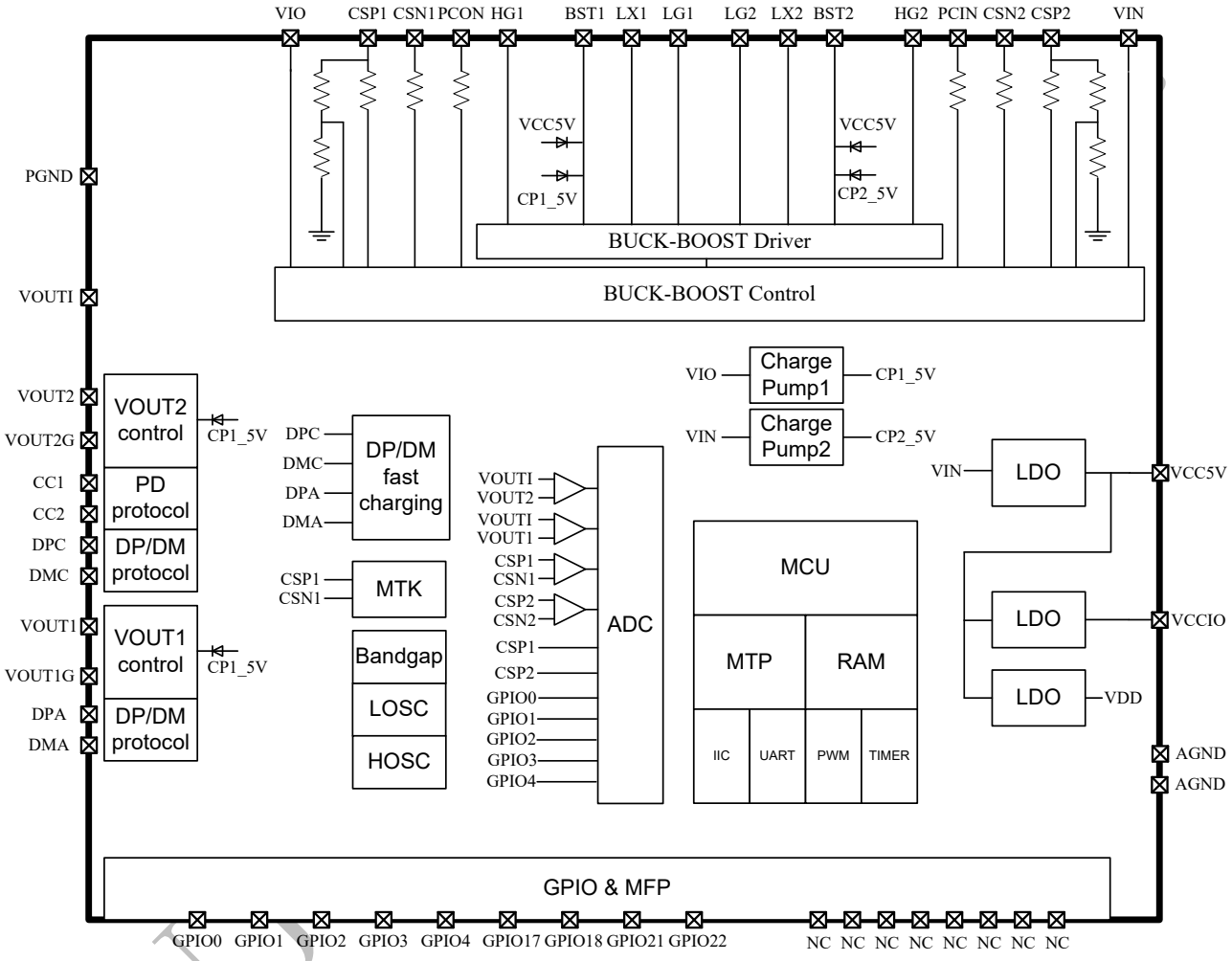


Figure3 IP6559 Internal block diagram

Synchronized Switch Buck-Boost Driver

IP6559 integrates a synchronized switch buck-boost driver, wide input voltage ranges from 3.6V to 31V and output from 3.0V to 20V.

IP6559 integrates input peak inductance current limiting and output average current limiting functions.

IP6559 output is driven at a switching frequency of 250kHz, It can be adjusted internally.

IP6559 has soft start function, preventing the huge inrush current cause damage to the IC. When VIN=12V, VOUT=5V, the soft start time is 4.75ms.

The MOSFET $R_{DS(ON)}$ = 3.6mohm@$V_{GS} = 10V$ When VIN=12V, VOUT2=5V@5A, the conversion efficiency is 95%.

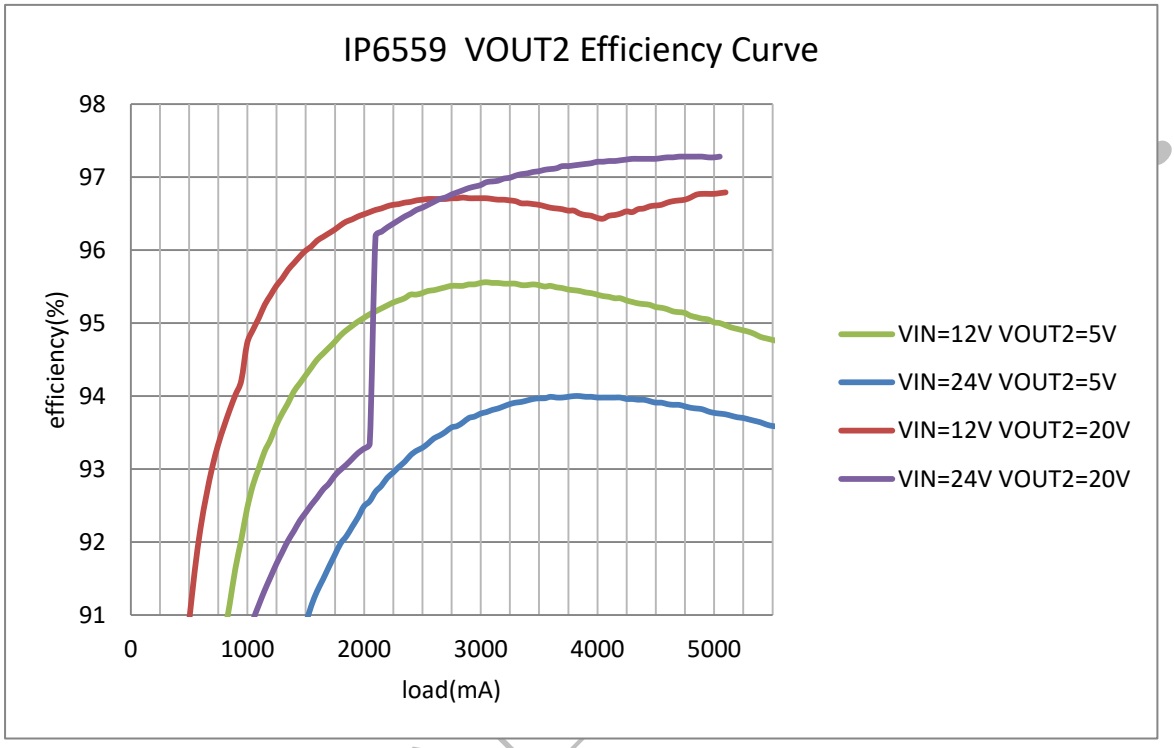


Figure 4. IP6559 VOS1 output efficiency curve

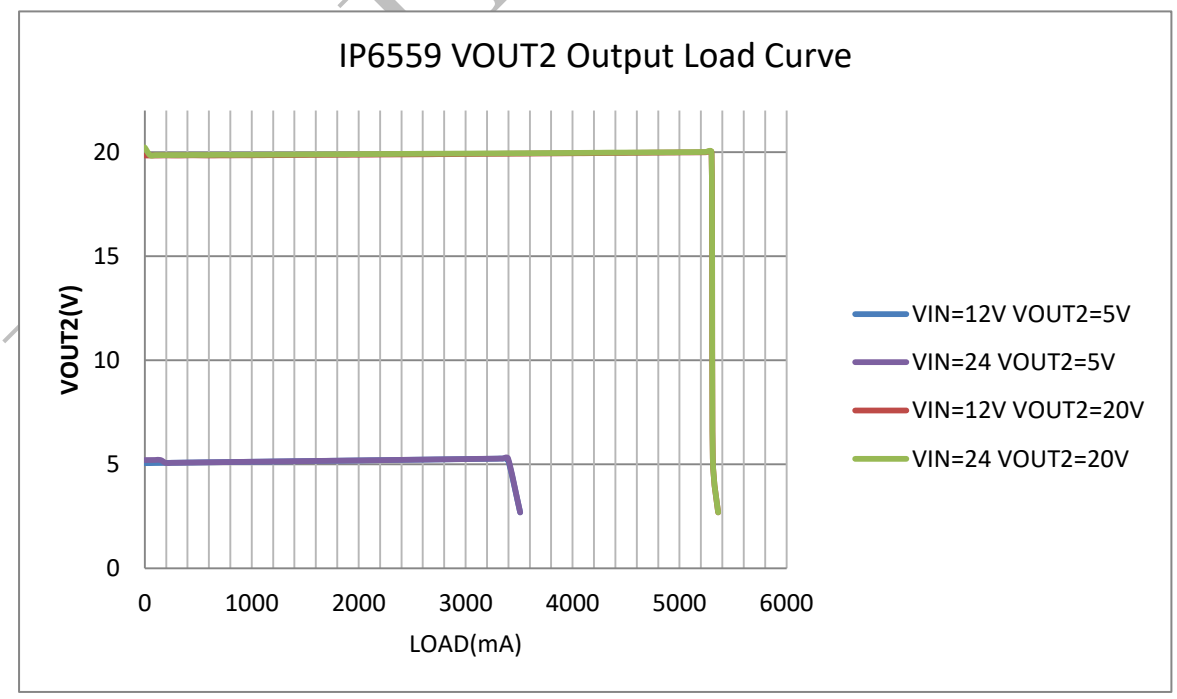


Figure 5. IP6559 VOUT2 output load curve

Output Voltage Line Compensate

IP6559 supports output line compensate, output voltage will increase about 30mV as output current increase 1A.

Output CV/CC Characteristic

IP6559 output has CV/CC mode: when the output current is lower than preset value, the output is in CV mode with constant voltage; when the output current is higher than preset value, the output is in CC mode with decreasing output voltage. The load current continues to increase and the output voltage rapidly decreases until the output voltage undervoltage protection is triggered.

Output CC Current Set

IP6559 output current limit can be adjusted by regulate the 5mohm sensing resistor between CSP1 and CSN1. The load current is measured by detect the voltage drop between CSP1 and CSN1.

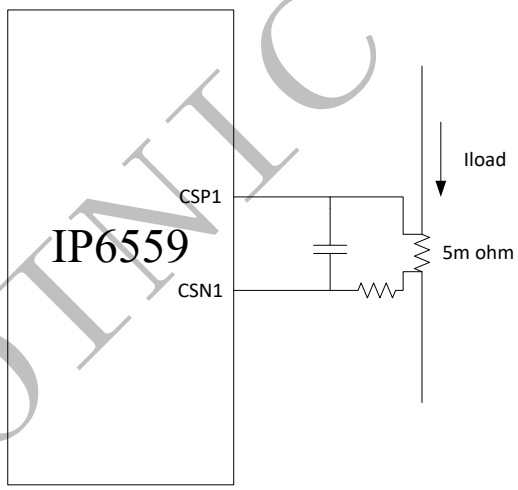


Figure 6. IP6559 output current limiting circuit

When the value of 5mohm current detect resistor is changed, the IP6559 output current limit will be changed accordingly.

In PCB layout, pay attention to the trace routing of CSP1 and CSN1, the trace should go out directly from the two side of 5mOhm resistor, avoiding introduce current limit deviation because of additional PCB trace resistor. Other than that, the 5mohm resistor should use alloy resistor with good temperature coefficient (100ppm) and high precision of 1%.

Protection Function

IP6559 will detect the VIN voltage, if VIN voltage is lower than 3.6V, IP6559 will enter standby mode and shut down the output.

IP6559 supports input over voltage protection: when the VIN voltage is higher than 31V, IP6559 determines the VIN is over voltage and shutdown the output; when VIN decrease under 29V, IP6559 determines the input voltage recovers and opens the output.

IP6559 supports output under voltage protection: if the VOUT voltage is lower than 2.6V, IP6559 determines the output is under voltage and will shut down the output and hiccup restart after 2sec.

IP6559 supports short circuit protect, 24ms after the circuit is started, if VOUT voltage is under 2.6V, IP6559 determines the output is short circuit and will shut down the output and hiccup restart after 2sec.

IP6559 supports over temperature protection: when the temperature detected is higher than 150℃, the output will be shut down. When the temperature decreases below 110℃, IP6559 determines the temperature has recovered and will restart the output.

Dual Output Ports

IP6559 supports two USB A or USBA+USBC output ports, either port supports fast charge output. Dual ports output power is 5V when two ports are connected to devices.

When dual ports have attached device, dual ports overall output power is 5V/4.8A.

IP6559 integrates dual ports automatic detection of device plug-in and plug-out detection function, either port can support fast charge output.

IP6559 uses a combination of voltage, current and protocol for device plug-in and plug-out detection.

EN PIN Function

IP6559 supports EN PIN to control the device on and off.

There is internal pull up of the EN PIN, and the DCDC function is enabled when EN PIN is high level, the DCDC function is disabled when EN PIN is low level.

Voltage and Current Acquisition and Display

IP6559 integrates built-in 14-bit ADC to accurately measure the voltage and current of the input and output, and supports display function.

IP6559 GPIO integrates analog input function, it can be used to measure the voltage or current.

Fast Charge Protocol Output

IP6559 supports fast charge protocol output, the specifications are as follows:

- ✧ Support Type-C and PD2.0/PD3.0(PPS) protocol

- ✧ Support BC1.2 and Apple protocol
- ✧ Support QC2.0/ QC3.0/ QC3+ protocol
- ✧ Support FCP/SCP protocol
- ✧ Support AFC protocol
- ✧ Support VOOC protocol

Note: The standard product IP6559 does not support the VOOC protocol;

The customer can apply for a customized part number that supports the VOOC protocol after the customer obtains the VOOC authorization.

10 Application Notes

Input Capacitance Selection

The ESR of the input capacitor should be as small as possible. The ESR will affect the conversion efficiency of the system.

When the input voltage is significantly greater than the output voltage, the device works in buck mode. The maximum ripple current supported by the input capacitor must be greater than the maximum VIN ripple current of the system. The ripple current RMS value ($I_{RMS(VIN)}$) of the input capacitor is calculated as follows:

$$I_{RMS(VIN)} = I_{LOAD} * \sqrt{\frac{V_{OUT}}{V_{IN}} * (1 - \frac{V_{OUT}}{V_{IN}})}$$

I_{LOAD} is the load current, V_{IN} is the input voltage, V_{OUT} is the output voltage.

Inductance Selection

The inductor with 10uH is recommended for most applications.

The DCR of inductor has great influence on the conversion efficiency of the system, low DCR inductors are recommended. For solutions above 30W, it is recommended to use an inductor with a DCR of less than 10mohm.

The inductor saturation current should be at least 20% greater than the system's peak inductor current limit, In order to avoid inductance saturation, resulting in a decrease in inductance, system instability.

The calculation formula of the PEAK current ($I_{L(PEAK)-BUCK}$) in buck mode is as follows:

$$I_{L(PEAK)-BUCK} = I_{LOAD} + \frac{V_{OUT}*(V_{IN}-V_{OUT})}{2*V_{IN}*F_S*L}$$

The calculation formula of the PEAK current ($I_{L(PEAK)-BOOST}$) in boost mode is as follows:

$$I_{L(PEAK)-BOOST} = \frac{V_{OUT}*I_{LOAD}}{V_{IN}*EFF} + \frac{V_{IN}*(V_{OUT}-V_{IN})}{2*V_{OUT}*F_S*L}$$

I_{LOAD} is the LOAD current, V_{IN} is the input voltage, V_{OUT} is the output voltage, L is the inductance, F_S is the switching frequency, EFF is the conversion efficiency of DCDC.

Output Capacitance Selection

When the output voltage is significantly greater than the input voltage, the device works in boost mode. The maximum ripple current supported by the output capacitor must be greater than the maximum VOUT ripple current of the system. The ripple current RMS value ($I_{RMS(VOUT)}$) of the output capacitor is calculated as follows:

$$I_{RMS(VOUT)} = I_{LOAD} * \sqrt{\frac{V_{OUT}}{V_{IN}} - 1)}$$

I_{LOAD} is the load current, V_{IN} is the input voltage, V_{OUT} is the output voltage.

The output capacitance is used to keep the output stable. The value of ESR and capacitance has an effect on the output ripple.

The output ripple voltage $V_{OUT(RIPPLE)-BUCK}$ in buck mode can be calculated as follows:

$$V_{OUT(RIPPLE)-BUCK} = \frac{V_{OUT}*(V_{IN}-V_{OUT})}{V_{IN}*L*F_S} * (R_{ESR} + \frac{1}{8*F_S*C_{OUT}})$$

R_{ESR} is the equivalent serial resistance value of the output capacitance, F_S is the switching frequency, C_{OUT} is the output capacitance value.

The output ripple voltage $V_{OUT(RIPPLE)-BOOST}$ in boost mode can be calculated as follows:

$$V_{OUT(RIPPLE)-BOOST} = \frac{I_{LOAD}*V_{OUT}*R_{ESR}}{V_{IN}} + \frac{(V_{OUT}-V_{IN})*I_{LOAD}}{V_{OUT}*F_S*C_{OUT}}$$

R_{ESR} is the equivalent serial resistance value of the output capacitance, F_S is the switching frequency, C_{OUT} is the output capacitance value.

MOSFET Selection

It is recommended to choose a $V_{(BR)DSS}$ MOSFET device with at least 20% higher than the input voltage.

$R_{DS(ON)}$ of MOSFET leads to the power loss of the on-device, which has a direct impact ON the conversion efficiency of the system. Generally, it is recommended to choose a 10mohm MOSFET with $R_{DS(ON)}$.
If the solution requires higher power output, lower $R_{DS(ON)}$ devices are recommended.

The C_{ISS} of MOSFET affects its switching speed. It is necessary to adjust the resistance of HG and LG in series according to different MOSFET, and adjust the driving speed of MOSFET to ensure the system stability.

It are advised to choose the MOSFET which C_{ISS} value is less than 1000pF.

The RC buffer circuit of LX1/LX2 can suppress the burr of LX. The proper RC buffer circuit can make the system have better EMI effect.

For the circuit of the driving part, it is recommended to reserve HG1/HG2 and LG1/LG2 series resistors of 0603 specifications and RC buffer circuit as shown in the following figure.

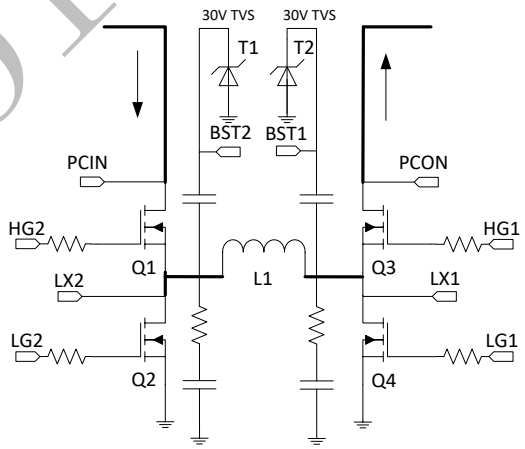


Figure 7. IP6559 MOSFET drive circuit diagram

11 Typical Application Schematic

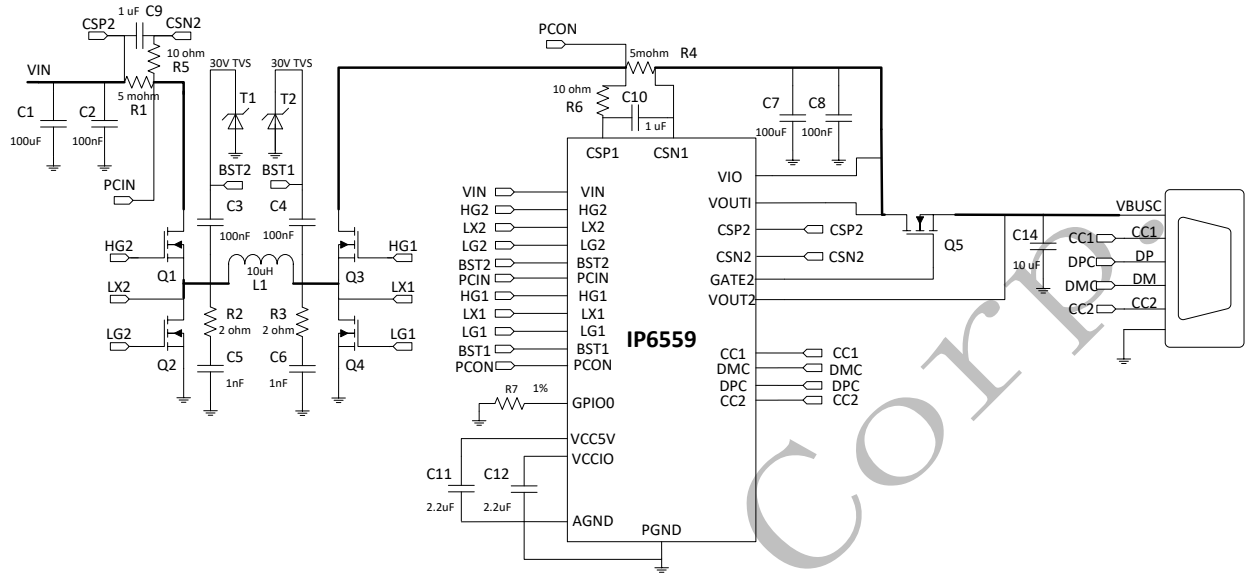


Figure 8. Typical application schematic diagram of IP6559 single C port

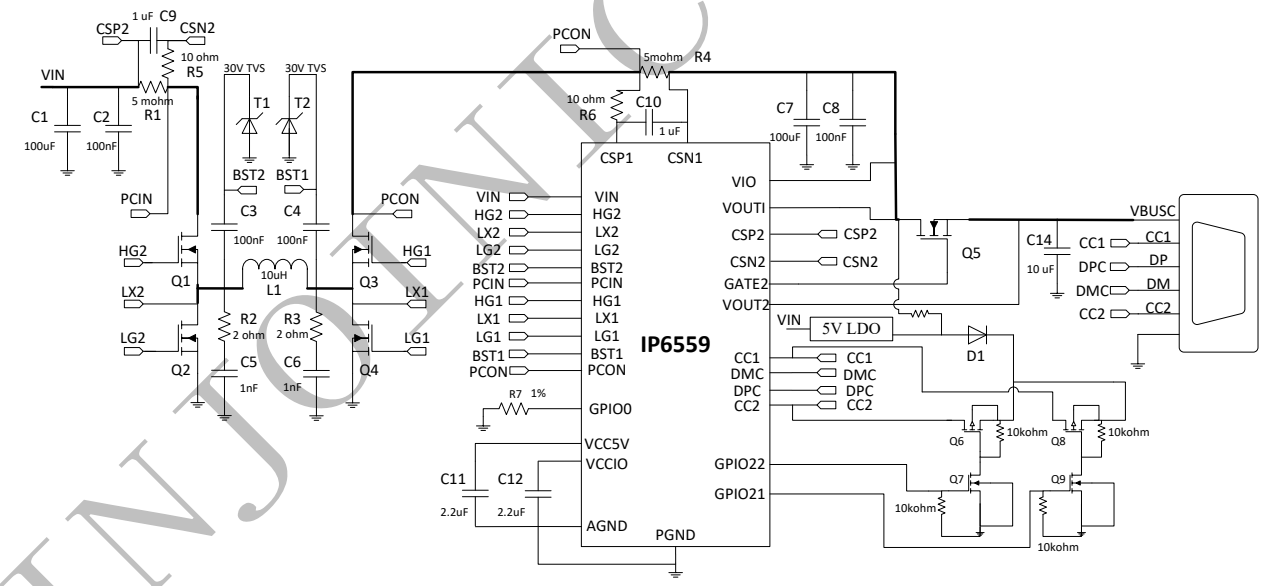


Figure 9. Typical application schematic diagram of IP6559 single C port with EMARK identification output

Notes:

1. In Figure 8 and Figure 9, adjusting the resistance R7 can change the PDO of IP6559_C port C;

2. In Figure 10, adjusting the resistance R7 can change the PDO of IP6559_C port C, and adjusting the resistance R8 can Change the output power of IP6559_C port A;

3. In Figure 11, adjusting the ground resistance R10/R11/R12 can change the PDO of IP6559 port C in different states of the dual ports; If you don't want to reduce power in corresponding state, the R11 or R12 is not need;

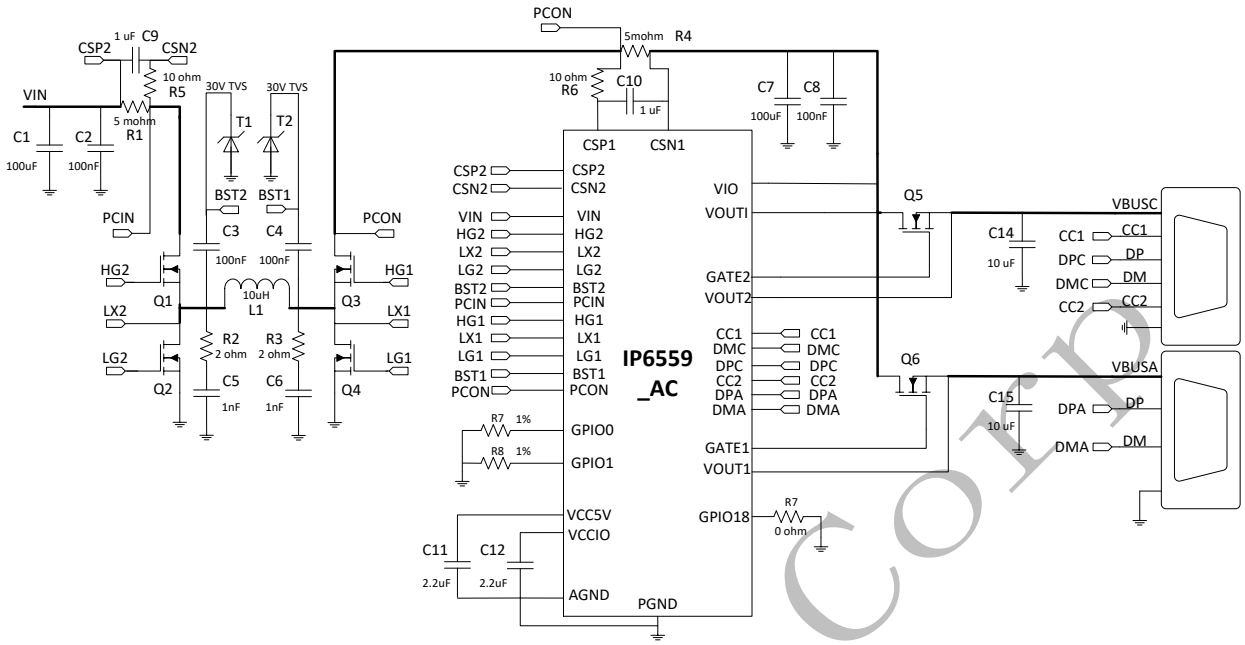


Figure 10. Typical application schematic diagram of IP6559 USBA and USBC dual-port output

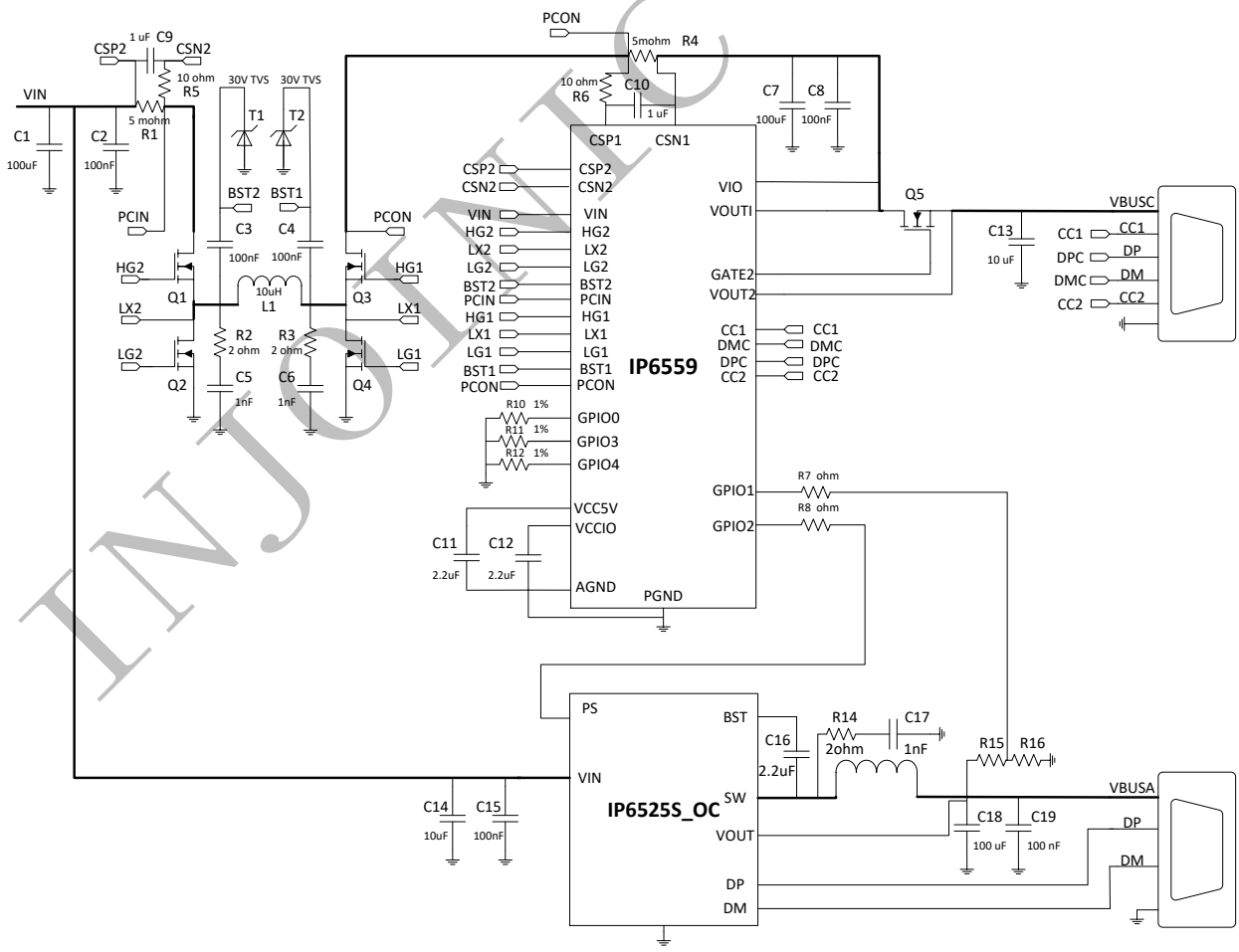


Figure 11. Typical application schematic diagram of IP6559 +IP6525S_OC dual-port with intelligent adjustment

12 BOM List

With the application of IP6559_C single USBC output port with digital tube display output , the finished BOM is as follows:

No.	Part Name	Type	Unit	Qty	Location	Notes
1	IC	IP6559_C	PCS	1		
2	Inductor	10uH+/-20%, current 10A DCR<10mohm	PCS	1	L1	
3	Electrolytic capacitor	100uF	PCS	1	C1	Withstand voltage higher than 35V
4	SMD capacitor	0603 100nF 10%	PCS	1	C2	Withstand voltage higher than 35V
5	SMD capacitor	0603 100nF 10%	PCS	3	C3, C4, C13	Withstand voltage higher than 16V
6	SMD capacitor	0603 1nF 10%	PCS	2	C5, C6	Withstand voltage higher than 35V
7	Solid-state capacitor	100uF	PCS	1	C7	Withstand voltage higher than 25V
8	SMD capacitor	0603 100nF 10%	PCS	1	C8	Withstand voltage higher than 25V
9	SMD capacitor	0603 1uF 10%	PCS	2	C9, C10	Withstand voltage higher than 16V
10	SMD capacitor	0603 2.2uF 10%	PCS	2	C11, C12	Withstand voltage higher than 16V
11	SMD capacitor	0603 10uF 10%	PCS	1	C14	Withstand voltage higher than 25V
12	SMD resistor	1206 5mohm 1% precision, temperature coefficient less than 100ppm	PCS	2	R1、R4	Current sense resistor
13	SMD resistor	0603 2R 5%	PCS	2	R2, R3	
14	SMD resistor	0603 10R 5%	PCS	2	R5, R6	
15	SMD resistor	0603 1%	PCS	1	R7	
16	MOSFET	MOSFET	PCS	5	Q1, Q2, Q3, Q4, Q5	
17	TVS	30V TVS	PCS	2	T1, T2	

13 Precautions for PCB layout

IP6559 integrates step-down controller. PCB layout is important for system stability, EMI, and other performance indicators. The PCB layout suggestions are as follows:

1. The loop composed of input capacitor and upper tube NMOS (controlled by HG2) and lower tube NMOS(controlled by LG2) should be as small as possible;

2. The loop composed of output capacitor and upper tube NMOS (controlled by HG1) and lower tube NMOS(controlled by LG1) should be as small as possible;

3. The inductor cable connecting the upper power tube and the lower power tube should be as wide and short as possible, so that the node area can ensure the maximum output current capacity;

4. The loop composed of LX1/LX2 buffer circuit and PGND should be as small as possible;

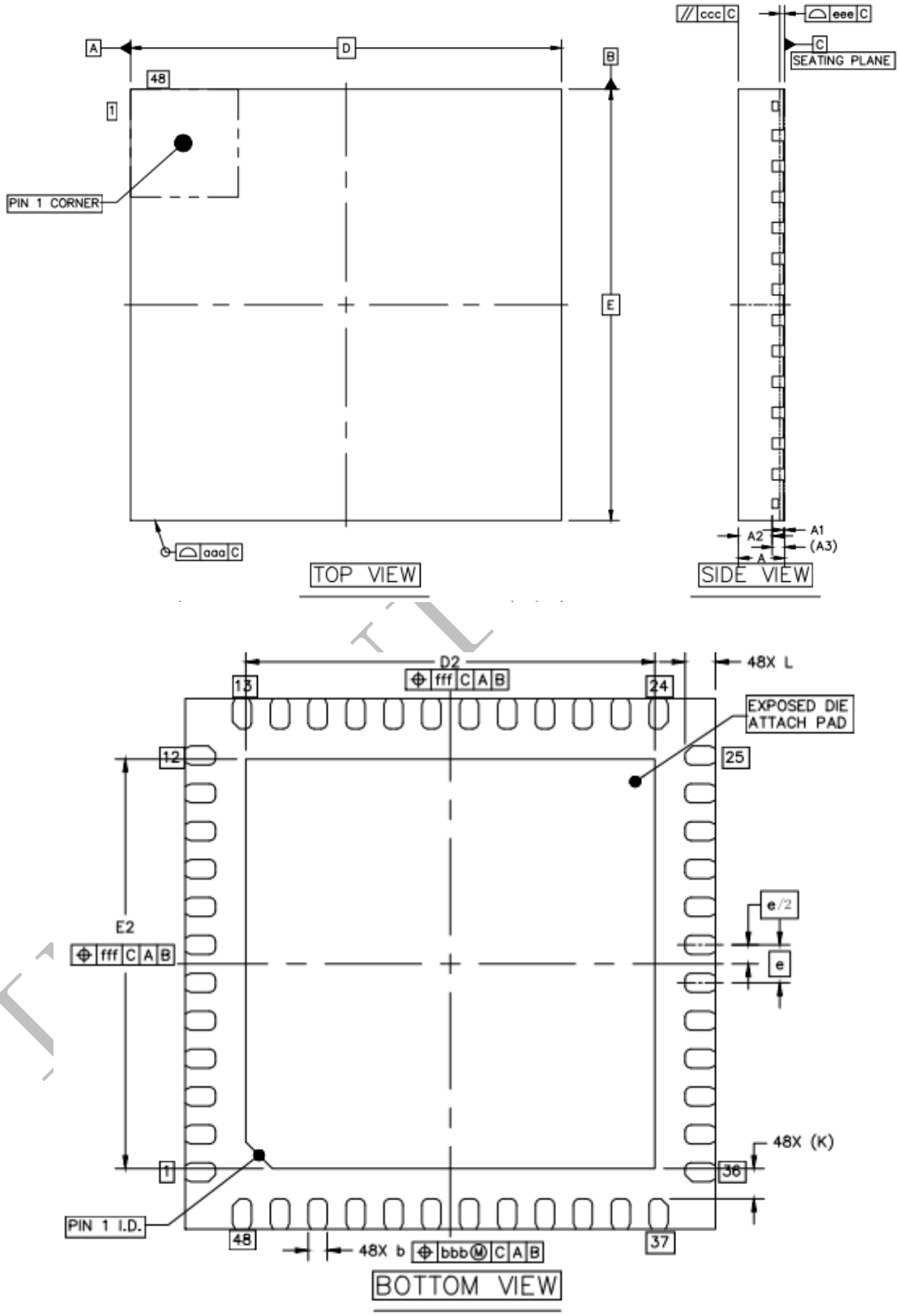
5. The current sampling line for 5mohm resistance is directly drawn from both ends of the resistance（including PCON/CSP2/CSN2/PCIN/CSP1/CSN1）. The line is parallel, as short as possible and avoids SW and other nodes;

6. The capacitance of VCC5V and VCCIO is placed close to the device PIN;

7. The GND of the input and output capacitors must be connected to the PGND of a large area;

8. Please refer to the IP6559 Application Notes for further information.

14 Package



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.55	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D		7 BSC	
	Y	E		7 BSC	
LEAD PITCH		e		0.5 BSC	
EP SIZE	X	D2	5.3	5.4	5.5
	Y	E2	5.3	5.4	5.5
LEAD LENGTH		L	0.3	0.4	0.5
LEAD TIP TO EXPOSED PAD EDGE		K		0.4 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.08	
LEAD OFFSET		bbb		0.1	
EXPOSED PAD OFFSET		fff		0.1	

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