

## Output 45W Power Buck SOC with Multiple Fast Charge Protocols

### 1 Features

- AEC-Q100 Qualified for Automotive Applications
  - Temperature grade 2: -40°C ~ +105°C
- Synchronous Step-Down Converter
  - Built-in Power MOSFETs
  - Input voltage range: 7.3V to 29.5V
  - Output voltage range: 3.0V to 21V
  - Output voltage line complement function
  - Output power support CV/CC mode
  - VIN=16V, VOUT=5V@3A, Conversion efficiency up to 93.7%
- Support Type-C Output and PD Protocol
  - Support 5V, 9V, 12V, 15V, 20V output
  - Support PD2.0/PD3.1 output protocol
  - PPS support 3.3V to 21V adjustable voltage with 20mV/step output
- Fast Charge Output
  - Support Type-C PD output
  - Support BC1.2 and Apple
  - Support QC2.0, QC3.0 and QC3+
  - Support Huawei Fast charge FCP
  - Support Samsung fast charge AFC
  - Support Universal fast charging UFCS
- Multi-Protection and High Reliability
  - Input overvoltage, input under voltage
  - Output short circuit, output overcurrent protection
  - Over temperature protection
  - DP/DM/CC over voltage protection
  - CC withstand voltage of 25V
  - HBM ESD 2KV
- Package: 4\*4mm QFN24

### 2 Application

- Automotive USB charging ports

### 3 Introduction

IP6529\_Q1 is a synchronized switch buck regulator which supports multiple fast charge output protocols, providing solutions for car charger and charge adaptor.

IP6529\_Q1 has built-in power MOSFET, input voltage range is 7.3V to 29.5V, output voltage ranges from 3V to 21V, and supply up to 45W output power, can automatically adjust the output voltage and current according to the identified fast charging protocol, typical output voltage and current are: 5V@3A, 9V@3A.

IP6529\_Q1 output power has CV/CC characteristic. When the output current is lower than the preset value, it is in CV mode with a constant output voltage; when the output current is higher than the preset value, it enters CC mode and the output voltage decreases as the output current increases.

IP6529\_Q1 has built-in 12-bit ADC, which can accurately measure input voltage, output voltage and current, and chip temperature, and can read output voltage and output current information through the IIC.

IP6529\_Q1 supports soft start, providing resistibility on the large inrush current during circuit start up.

IP6529\_Q1 supports multiple protection on input overvoltage and under voltage, output overcurrent, overvoltage, under voltage and short circuit.

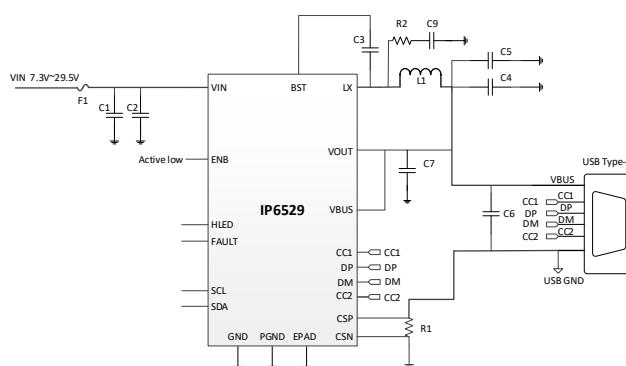


Fig.1 IP6529\_Q1 Simplified Application Schematic

## Content

1 Features .....	1
2 Application.....	1
3 Introduction .....	1
4 Revision History .....	3
5 Typical Application Schematic Diagram .....	4
6 PIN Definition .....	5
7 IP6529_Q1 Model Selection Table.....	6
8 Internal Block Diagram.....	7
9 Absolute Maximum Ratings.....	8
10 Recommended Operating Conditions .....	8
11 Electrical Characteristics .....	9
12 Function Description .....	11
12.1 Synchronized Switch Buck Regulator .....	11
12.2 Output Voltage Line Complement Function .....	12
12.3 Output CC/CV Characteristic .....	12
12.4 Output CC Current Set.....	12
12.5 Protections .....	13
12.6 Fast Charge Protocols.....	14
12.7 Type-C Port and USB PD Protocol.....	14
12.8 ENB PIN Function.....	14
12.9 HLED PIN Function .....	14
12.10 FAULT PIN Function .....	14
12.11 IIC Control and ADC .....	15
13 Application Notes.....	16
13.1 Input Capacitance Selection .....	16
13.2 Inductance Selection .....	16
13.3 Output Capacitance Selection .....	16
14 Typical Application Schematic .....	17
15 BOM .....	18
16 Considerations for PCB Layout .....	19
17 Package .....	20
18 Tape and Packaging Information.....	24
18.1 Tape Information .....	24
18.2 Reel Packaging Carton Specifications.....	25
19 Silk Screen Information .....	26
20 Photos of Physical Objects .....	26
IMPORTANT NOTICE .....	27

## 4 Revision History

Notes: The page number of the previous version may different from the page number of the current version

**Initial Release V 1.00 (Apr 2023)**

**Changes from Revision V1.00 (Apr 2023) to Revision V1.10(Oct 2023)**

- 
- 1、Change the schematic diagram and BOM
  - 2、Change the description of HLED and FAULT function.
- 

**Changes from Revision V1.10 (Oct 2023) to Revision V1.15 (Sep 2024)**

- 
- 1、Increase switching frequency gear: 330kHz (support customization)
- 

INJOINIC Corp.

## 5 Typical Application Schematic Diagram

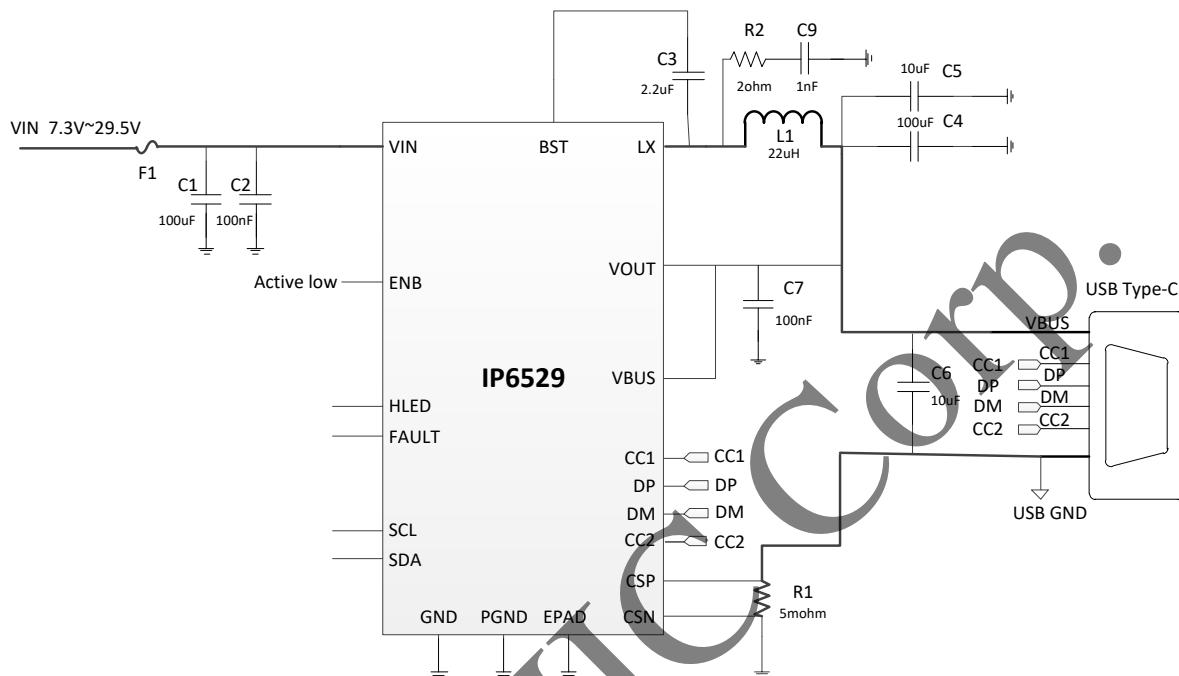


Fig. 2 IP6529\_Q1 Application Schematic of PD Fast Charging Output With External Sensing Resistor

Notes:

- (1) IP6529\_Q1 EPAD must have a good contact with PCB GND;
- (2) ENB cannot be suspended and needs to be given a definite level; the chip turns on when ENB is low and turns off when ENB is pulled up to 2V or more;
- (3) C1 and C2 should be placed close to the PIN2/PIN3 of IP6529\_Q1; C2 requires an appropriate increase in capacitance if it is far from the 100uF capacitor or the power supply VIN;
- (4) C7 and C8 should be placed close to the PIN18/PIN19 of IP6529\_Q1;
- (5) R2 and C9 should be placed close to the LX (PIN22/PIN23/PIN24) of IP6529\_Q1, and the loop composed of LX pin, R2, C9 and PGND should be minimized on the PCB board;
- (6) When the USB port on the program does not use DP and DM pin, the DP and DM interface should be reserved on the PCB to facilitate subsequent upgrades of the device.

## 6 PIN Definition

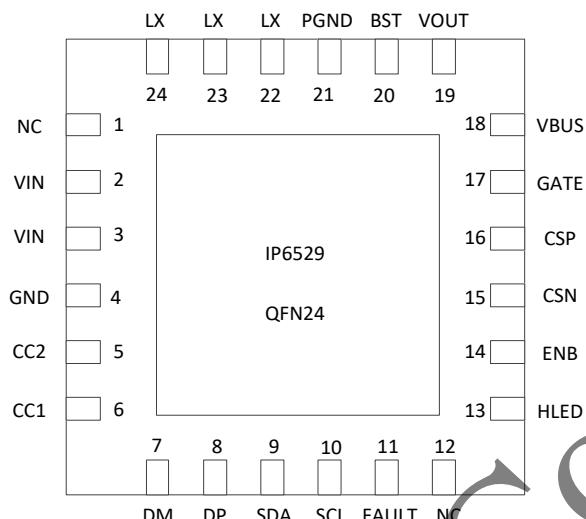


Fig. 3 IP6529\_Q1 PIN Configuration

Pins		Description
Pin NO.	Pin Name	
1/12	NC	NC pin
2/3	VIN	Input voltage node
4	GND	System ground
5	CC2	USB C port detection and fast charge communication pin CC2
6	CC1	USB C port detection and fast charge communication pin CC1
7	DM	USB C port fast charge communication pin DM
8	DP	USB C port fast charge communication pin DP
9	SDA	IIC serial interface data input/output pin
10	SCL	IIC serial interface clock input pin
11	FAULT	Abnormal status indication pin
13	HLED	Fast charge output indication pin
14	ENB	Chip enable pin, cannot be suspended. Chip enable when ENB is pulled low externally.
15	CSN	Output Current sampling negative terminal
16	CSP	Output Current sampling positive terminal
17	GATE	Output path MOS driver pin
18	VBUS	VBUS voltage detection pin
19	VOUT	VOUT voltage feedback pin
20	BST	Bootstrap capacitor pins
21	PGND	Power ground
22/23/24	LX	Power switch node, connected to external inductor
25	EPAD	Power ground

## 7 IP6529\_Q1 Model Selection Table

Product	USB	Output Power		
		PDO	5V/3A	9V/3A
IP6529_Q1	USB Type-C	QC	5V/3A	9V/2A
		-	-	-

Notes:

1. IP6529\_Q1 supports a maximum power output of 45W (20V/2.25A).
2. The FAULT and HLED Pins of the IP6529\_Q1 can be multiplexed for other functions as required.
3. The switching frequency of IP6529\_Q1 can be customized to 115KHz/330kHz according to requirements.

## 8 Internal Block Diagram

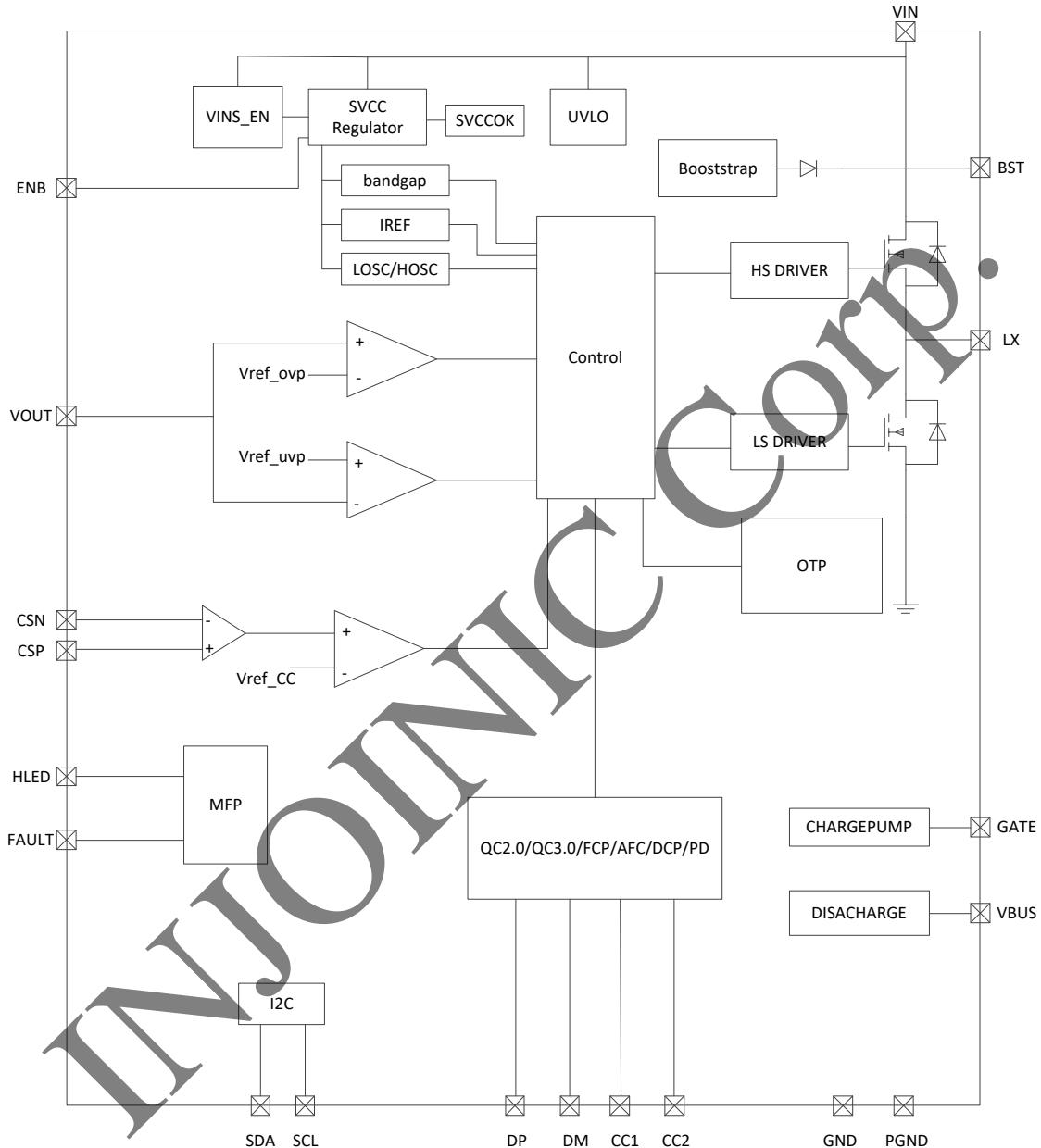


Fig. 4 IP6529\_Q1 Internal Block Diagram

## 9 Absolute Maximum Ratings

Parameters	Symbol	Value	Unit
Input voltage range	$V_{IN}$	-0.3 ~ 36	V
LX voltage range	$V_{LX}$	-0.3 ~ $V_{IN}+0.3$	V
VOUT voltage range	$V_{VOUT}$	-0.3 ~ 25	V
DP/DM/CC voltage range	$V_{DP/DM/CC1/CC2}$	-0.3 ~ 22	V
Junction Temp range	$T_J$	-40 ~ 150	°C
Storage Temp range	$T_{STG}$	-60 ~ 150	°C
Operating ambient temperature range	$T_A$	-40 ~ 105	°C
Thermal resistance (junction to ambient)	$\theta_{JA}$	50	°C/W
ESD (HBM)	ESD	2	kV

\* Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to Absolute Maximum Rated conditions for extended periods may affect device reliability.

## 10 Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input voltage	$V_{IN}$	7.3	16	29.5	V

\*Devices' performance cannot be guaranteed when working beyond those Recommended Operating Conditions

## 11 Electrical Characteristics

Unless otherwise specified, TA=-40~+105°C, L=22uH, VIN=16V, VOUT=5V, tested on the IP6529\_Q1 demo.

Parameters	Symbol	Test Condition	Min.	Typ.	Max	Unit
<b>Input system</b>						
Input voltage	V <sub>IN</sub>		7.3	16	29.5	V
Input under voltage	V <sub>IN-UV</sub>	Rising voltage	7.1	7.2	7.3	V
	V <sub>IN-UV-TH</sub>	Falling voltage	-	0.3	-	V
Input over voltage	V <sub>IN-OV</sub>	Rising voltage	29.3	29.5	29.8	V
	V <sub>IN-OV-TH</sub>	Falling voltage	-	0.2	-	V
Input quiescent current	I <sub>Q</sub>	VIN=16V, Standby status	-	0.55	-	mA
Shutdown current	I <sub>SD</sub>	Input current at ENB=3.3V, VIN=16V	-	15	-	uA
<b>Power switching system</b>						
High-side MOS Ron resistance	R <sub>DSON_L</sub>		-	30	-	mΩ
Low-side MOS Ron resistance	R <sub>DSON_H</sub>		-	20	-	mΩ
Maximum Duty Cycle	D <sub>MAX</sub>	VIN = 9V, VOUT = 9V/3A	-	95	-	%
Switching frequency	F <sub>S</sub>		100	115	130	KHz
Switching frequency(optional)	F <sub>S_1</sub>		310	330	350	KHz
<b>Output system</b>						
Output voltage	V <sub>OUT</sub>		3	5	21	V
Output voltage ripple	ΔV <sub>OUT</sub>	VIN = 16V, VOUT=5V/3A	75	85	100	mV
		VIN = 16V, VOUT=9V/3A	85	90	100	mV
Note: Typical values tested under the demo board reference design						
Soft start time	T <sub>SS</sub>	VIN = 16V, VOUT = 5V	-	8	-	ms
Output line compensate voltage	V <sub>COMP</sub>	VIN = 16V, VOUT = 5V, I <sub>OUT</sub> = 3A	-	150	-	mV
Max output current in CC mode (IP6529_Q1)	I <sub>OUT</sub>	VIN = 16V, VOUT = 5V	-15%	3	+15%	A
		VIN = 16V, VOUT = 9V	-15%	3	+15%	A
Output hiccup restart voltage	V <sub>OUT</sub>	Hiccup restart voltage when output enter CC mode(V <sub>OUT</sub> preset)	-	4.1	-	V

		voltage >= 5V)					
Output hiccup restart voltage	V <sub>OUT</sub>	Hiccup restart voltage when output enter CC mode (V <sub>OUT</sub> preset voltage < 5V)	-	3	-	V	
Output hiccup restart time	T <sub>HIC</sub>	VIN=16V, V <sub>OUT</sub> short circuit	-	2	-	s	
DPDM over voltage protection voltage	V <sub>OVP_DPD</sub> M	VIN = 16V, V <sub>OUT</sub> =5V	-	4.5	-	V	
CC over voltage protection voltage	V <sub>OVP_CC</sub>	VIN = 16V, V <sub>OUT</sub> =5V	-	6.0	-	V	
Thermal shutdown temperature	T <sub>OTP</sub>	Rising temperature	-	165	-	°C	
Thermal shutdown temperature hysteresis	ΔT <sub>OTP</sub>		-	10	-	°C	

**ENB PIN**

ENB Input shutdown voltage	V <sub>ENB-OFF</sub>	Input voltage of ENB rises to turn the device off	2	-	-	V
ENB Input turn-on voltage	V <sub>ENB-ON</sub>	Input voltage of ENB drops to turn the device on	-	-	0.5	V
ENB Input turn-on delay time	T <sub>ENB-ON</sub>	Delay time form ENB input is low to DCDC on	-	170	-	ms
ENB Input shutdown delay time	T <sub>ENB-OFF</sub>	Delay time form ENB input is high to DCDC off	-	50	-	μs

## 12 Function Description

### 12.1 Synchronized Switch Buck Regulator

IP6529\_Q1 integrates a high efficiency synchronous switching buck converter, which supports a wide input voltage range of 7.3V to 29.5V, and an output voltage range of 3.0V to 21V.

IP6529\_Q1 integrate power switch MOSFET with 115kHz working frequency.

The conversion efficiency is up to 93.7% at VIN=16V, VOUT=5V@3A. The efficiency under different input voltage and load current is shown in Fig. 5. and Fig. 6 shows the output voltage characteristics under different load current.

IP6529\_Q1 automatically adjusts the output voltage and current based on the recognized fast charging protocol.

IP6529\_Q1 has a soft-start function to prevent malfunction caused by excessive inrush current at startup. Soft-start time is 8ms for VIN=16V and 5V no-load output.

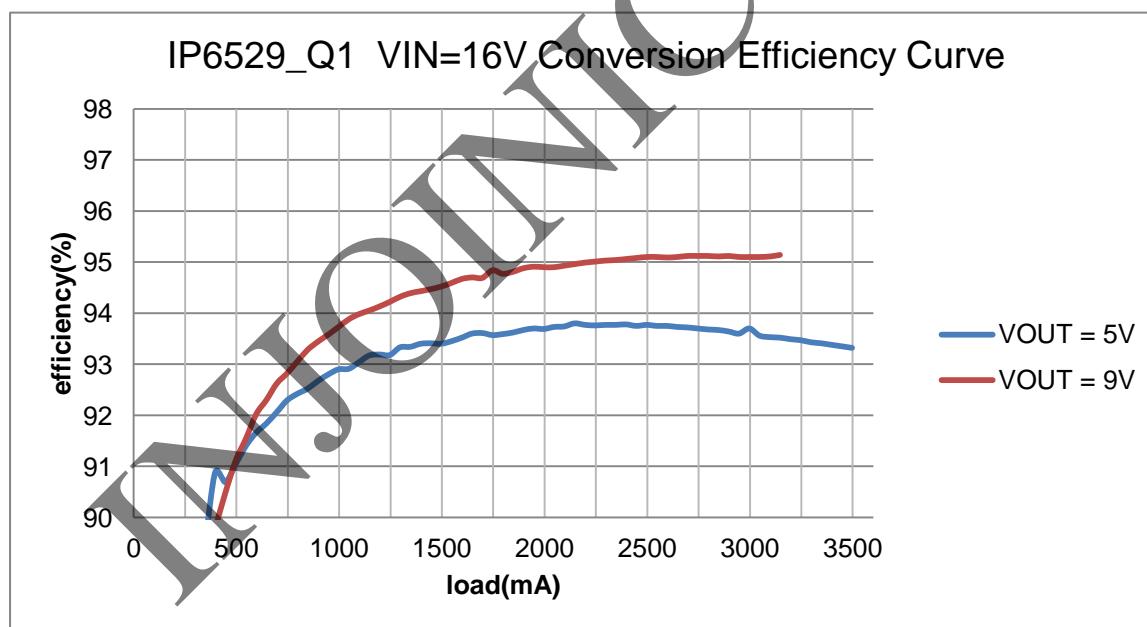


Fig. 5 IP6529\_Q1 Conversion Efficiency Curve

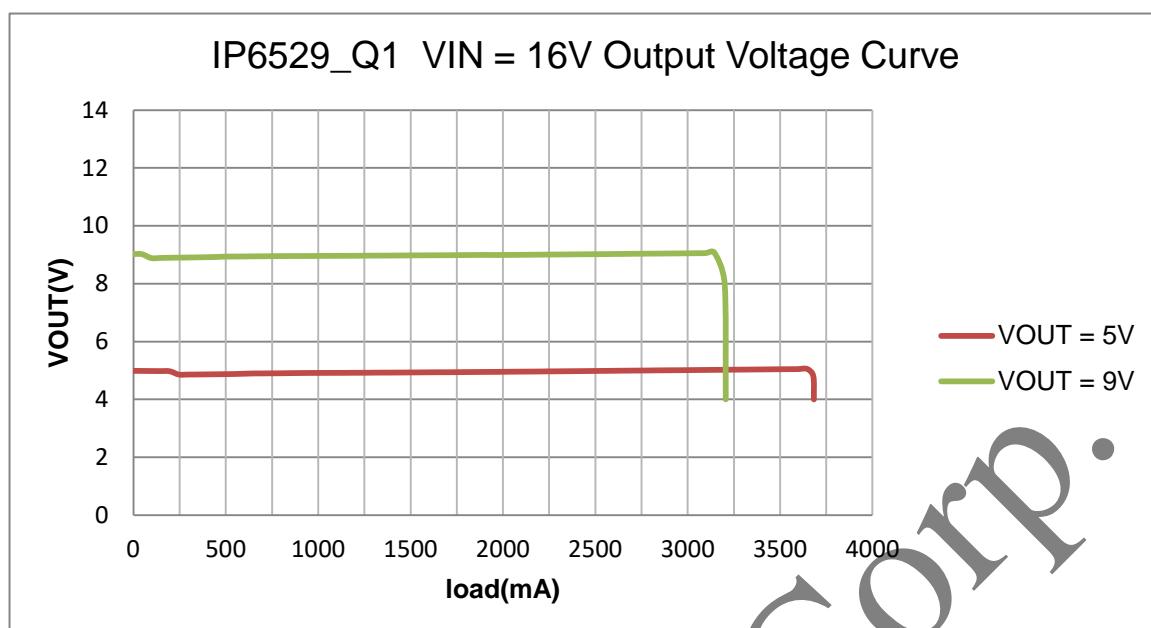


Fig. 6 IP6529\_Q1 Vout-Iout Curve when VIN=16V Output

## 12.2 Output Voltage Line Complement Function

IP6529\_Q1 supports output line compensate, output voltage will increase about 50mV as output current increases 1A.

## 12.3 Output CC/CV Characteristic

IP6529\_Q1 output power has CV/CC characteristic. when the output current is lower than the preset value, it is in CV mode with a constant output voltage; when the output current is higher than the preset value, it enters CC mode, and as the output current increases, the output voltage will decrease rapidly until the output voltage undervoltage protection is triggered;.

When VOUT preset voltage is higher or equal to 5V, if the load continues to increase, and output voltage is lower than 4.1V, the output will be shut down and hiccup restart after 2sec; When VOUT preset voltage is lower than 5V, if the load continues to increase, and output voltage is lower than 3V, the output will be shut down and hiccup restart after 2sec.

## 12.4 Output CC Current Set

IP6529\_Q1 output current limit can be adjusted by regulating the 5mohm sensing resistor between CSP and CSN. The voltage drops between CSP and CSN is detected to determine if the current load current is up to the preset current level.

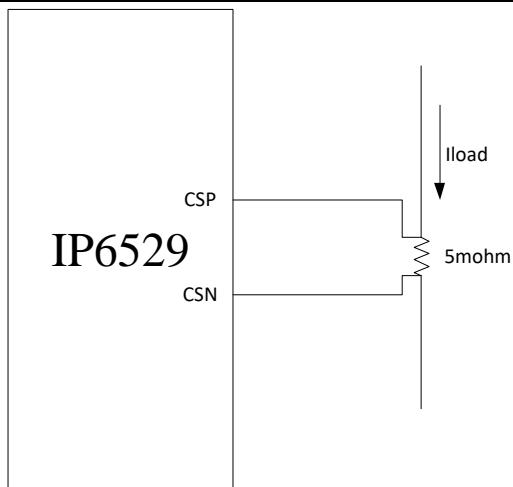


Fig. 7 IP6529\_Q1 Output Current Limiting Circuit

In PCB layout, pay attention to the trace routing of CSP and CSN, the trace should go out directly from the two sides of 5mOhm resistor, avoiding introduce current limit deviation because of additional PCB trace resistor.

Other than that, the 5mohm resistor should use alloy resistor with good temperature coefficient (100ppm) and high precision of 1%. When the value of 5mohm current detect resistor is changed, the IP6529\_Q1 output current limit will be changed accordingly.

## 12.5 Protections

IP6529\_Q1 supports input undervoltage protection: When the VIN voltage is lower than 6.9V, IP6529\_Q1 detects the input undervoltage and turns off the output.

IP6529\_Q1 supports input over voltage protection: When the VIN voltage is higher than 29.5V, IP6529\_Q1 will turns off the output. When the VIN drops under 29.3V, IP6529\_Q1 will consider the VIN normal and turn on the output.

IP6529\_Q1 supports output under voltage protection: When VOUT preset voltage is higher or equal to 5V, if the VOUT voltage is lower than 4.1V, IP6529\_Q1 determines the output is under voltage and will turn off the output and hiccup restart after 2sec. When VOUT preset voltage is lower than 5V, if the output voltage is lower than 3V, the output will be turned off and hiccup restart after 2sec.

IP6529\_Q1 supports short circuit protection: 8ms after the circuit is started, if VOUT voltage is under 4.1V, IP6529\_Q1 determines the output is short circuit and will turn off the output and hiccup restart after 2sec.

IP6529\_Q1 supports DP/DM/CC over voltage protection, when DP/DM voltage is higher than 4.5V, or CC1/CC2 voltage is higher than 6.0V, IP6529\_Q1 determines relevant signal PIN is over voltage and will turn off the output and hiccup restart after 2sec.

IP6529\_Q1 supports over temperature protection: when the temperature detected is higher than 165°C, the output will be turned off. When the temperature decreases below 155°C, IP6529\_Q1 determines the temperature has recovered and will restart the output.

## 12.6 Fast Charge Protocols

IP6529\_Q1 supports multiple fast charge protocols:

- Support DCP (BC1.2 and Apple)
- Support Qualcomm quick charge QC2.0, QC3.0 and QC3+
- Support Huawei FCP
- Support Samsung AFC (MAX 12V)
- Support Universal fast charging UFCS
- Supports Type-C output and USB PD2.0/PD3.0 (PPS) protocol

## 12.7 Type-C Port and USB PD Protocol

IP6529\_Q1 supports Type-C output and USB PD2.0/PD3.0 (PPS) protocol.

IP6529\_Q1 supports USB PD protocol output 27W; Package broadcast: 5V/3A, 9V/3A.

IP6529\_Q1 supports the standard Type-C specification and will not turn on the output until the CC connection is successful.

IP6529\_Q1 Type-C port detects the fast charge requirement automatically through DP/DM and CC1/CC2 pins and adjusts the output voltage and current accordingly.

## 12.8 ENB PIN Function

ENB is an external enable pin, which cannot be suspended and needs to be given a definite level; The chip turns on when ENB is low and turns off when ENB is pulled up to 2V or more;

ENB is 3.3V, the shutdown current at 16V input is 15uA.

ENB can not be connected to a high-voltage of 6V or more, otherwise it will cause this PIN overvoltage breakdown.

## 12.9 HLED PIN Function

HLED PIN of IP6529\_Q1 can be multiplexed as fast charging output indication function, as the following function description:

Used as fast charging output indication function, connects external light-emitting diode, Which will light up when QC and other high-voltage fast charging request voltage is not 5.0V, that is, the application voltage above or below 5.0V will light up; can be suspended when this function is not needed.

HLED PIN can not be connected to a high-voltage of 6V or more, otherwise it will cause this PIN over-voltage breakdown.

## 12.10 FAULT PIN Function

FAULT PIN supports open-drain output, which supports the indication of abnormal status such as input over-under voltage, over-temperature, DP/DM over-voltage, CC over-voltage, DM is shorted to GND, etc.

---

FAULT PIN can not be connected to a high-voltage of 6V or more, otherwise it will cause this PIN to over-voltage breakdown.

## 12.11 IIC Control and ADC

IP6529\_Q1 supports IIC control, as slave, external device can use IIC to control IP6529\_Q1 as needed.

IP6529\_Q1 built-in 12-bit ADC, can accurately measure the input voltage, output voltage, output current, and the ADC information can be read through IIC.

INJOINIC Corp.

## 13 Application Notes

### 13.1 Input Capacitance Selection

The ESR of the input capacitor should be as small as possible. The ESR will affect the conversion efficiency of the system.

The maximum ripple current supported by the input capacitor must be greater than the maximum VIN ripple current of the system. The ripple current RMS value of the input capacitor is calculated as follows:

$$I_{RMS} = I_{LOAD} * \sqrt{\frac{V_{OUT}}{V_{IN}} * (1 - \frac{V_{OUT}}{V_{IN}})}$$

$I_{LOAD}$  is the load current,  $V_{IN}$  is the input voltage,  $V_{OUT}$  is the output voltage.

### 13.2 Inductance Selection

The inductor with 22uH is recommended for most applications.

The DCR of inductor has a great influence on the conversion efficiency of the system, and low DCR inductors are recommended. For solutions above 30W, it is recommended to use an inductor with a DCR of less than 10mohm.

The inductor saturation current should be at least 20% greater than the system's peak inductor current limit to avoid inductor saturation, causing inductance drop and system instability.

The calculation formula of the PEAK current ( $I_L(PEAK)$ ) is as follows:

$$I_{L(PEAK)} = I_{LOAD} + \frac{\Delta I_L}{2}$$

$I_{LOAD}$  is the LOAD current,  $\Delta I_L$  is the peak-to-peak value of the inductor current, The calculation formula of  $\Delta I_L$  is as follows:

$$\Delta I_L = \frac{V_{OUT} * (V_{IN} - V_{OUT})}{V_{IN} * L * F_S}$$

$V_{IN}$  is the input voltage,  $V_{OUT}$  is the output voltage,  $L$  is the inductance,  $F_S$  is the switching frequency.

### 13.3 Output Capacitance Selection

The output capacitance is used to keep the output stable. The value of ESR and capacitance has an impact on the output ripple. The output ripple voltage  $V_{out-ripple}$  can be calculated as follows:

$$V_{out-ripple} = \Delta I_L * (R_{ESR} + \frac{1}{8 * F_S * C_{OUT}})$$

$\Delta I_L$  is the peak-to-peak value of the inductor current,  $R_{ESR}$  is the equivalent serial resistance value of the output capacitance,  $F_S$  is the switching frequency,  $C_{OUT}$  is the output capacitance value.

## 14 Typical Application Schematic

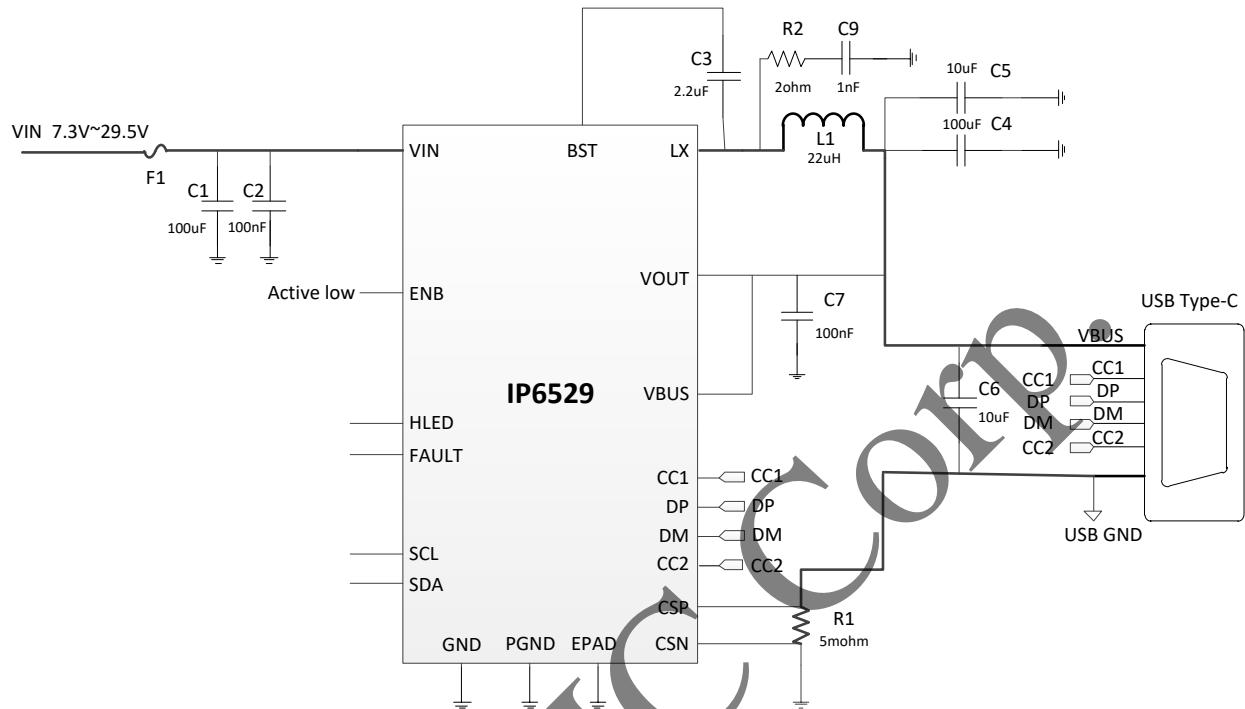


Fig. 8 IP6529\_Q1 Application Schematic of PD Fast Charging Output With External Sensing Resistor

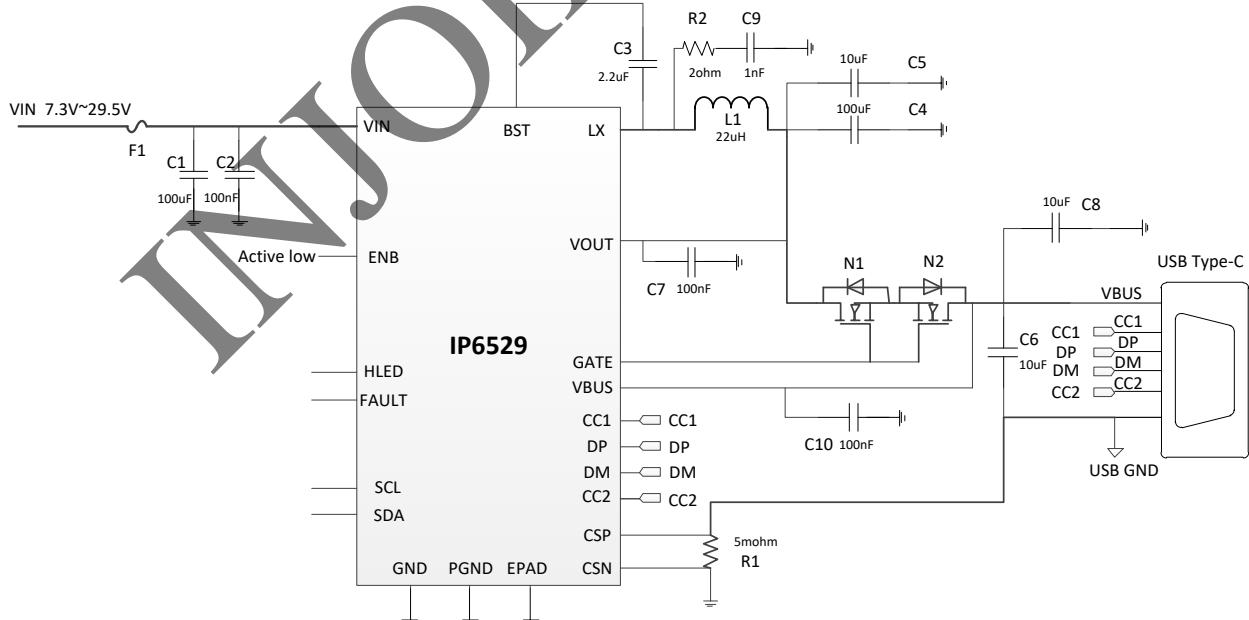


Fig. 9 IP6529\_Q1 Application Schematic with External Sensing Resistor and Path MOS

## 15 BOM

Taking IP6529\_Q1 DEMO as an example (Figure 9), the collated BOM list is as follows:

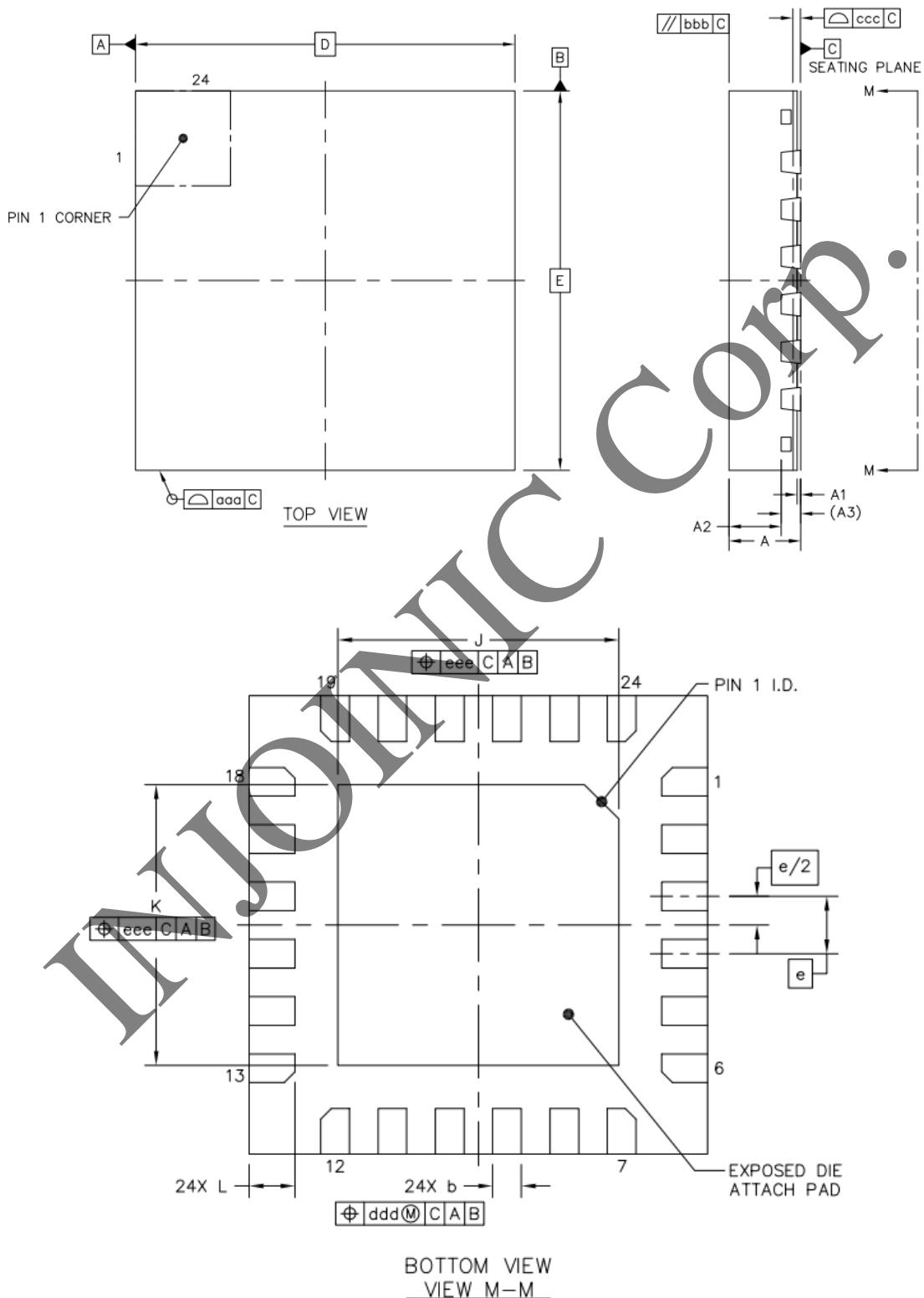
NO	Device	Spec.	Unit	Counts	Designator	备注
1	IC	IP6529_Q1	PCS	1		
2	magnetic ring inductor	22uH+/-20%, Nominal current 5A DCR<12mohm	PCS	1	L1	
3	electrolytic capacitor	100uF/35V	PCS	1	C1	Rated voltage>35V.
4	electrolytic capacitor	100uF/25V	PCS	1	C4	Rated voltage>25V
5	SMD capacitor	0603 100nF 10%	PCS	3	C2, C7, C10	Rated voltage>35V
6	SMD capacitor	0603 2.2uF 10%	PCS	1	C3	Rated voltage>35V
7	SMD capacitor	0603 1nF 10%	PCS	1	C9	Rated voltage>35V
8	SMD capacitor	0603 10uF 10%	PCS	3	C5, C6, C8	Rated voltage>25V
9	SMD resistor	0603 2R 5%	PCS	1	R2	
10	SMD resistor	1206 5mohm 1% precision, temperature coefficient less than 100ppm	PCS	1	R1	Current sense resistor
11	MOSFET	MOSFET	PCS	2	N1, N2	
12	Fuse		PCS	1	F1	

## 16 Considerations for PCB Layout

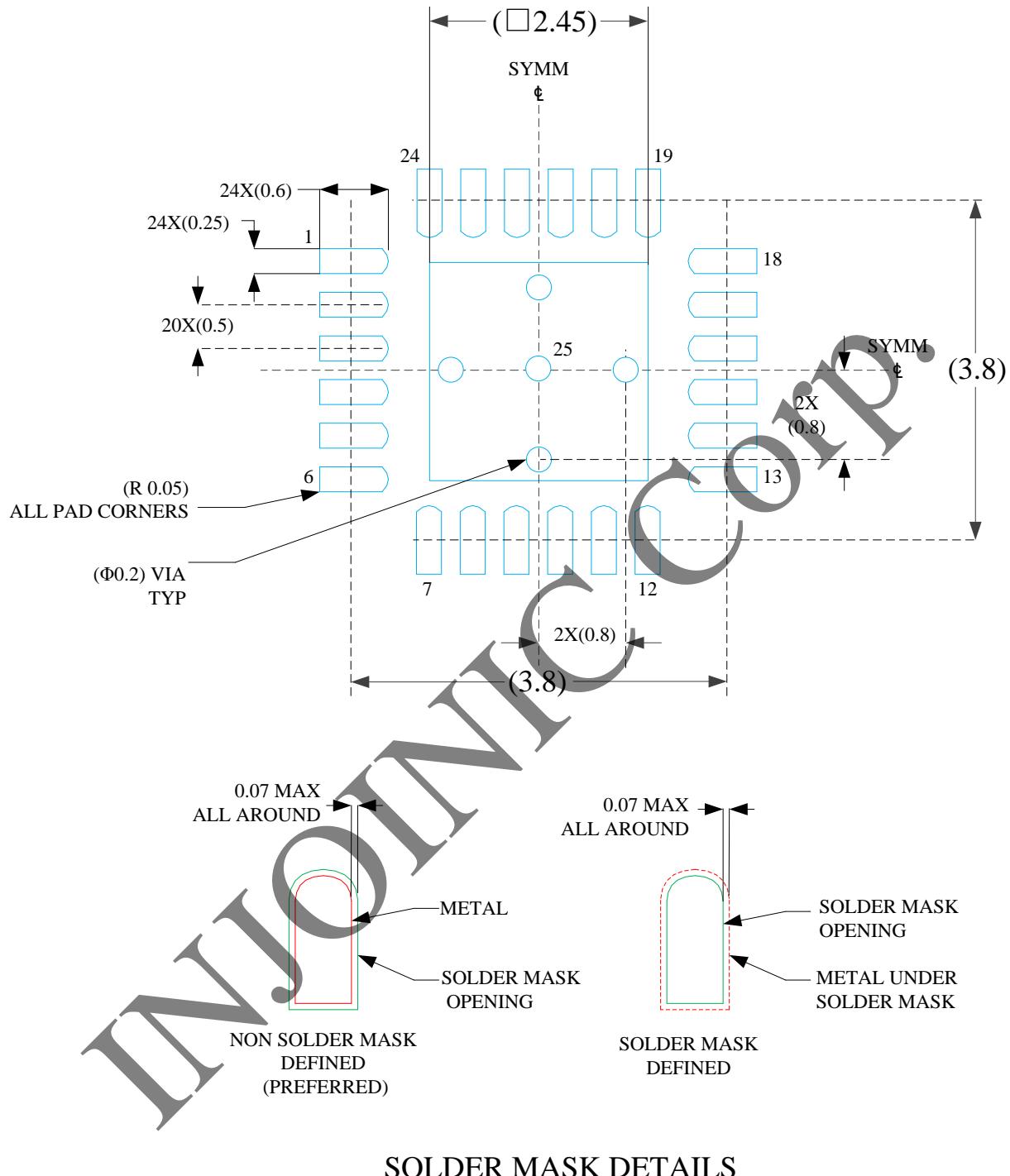
IP6529\_Q1 integrates buck converter, PCB layout is important for system stability, EMI, and other performance indicators, the IP6529\_Q1 PCB layout suggestions are as follows:

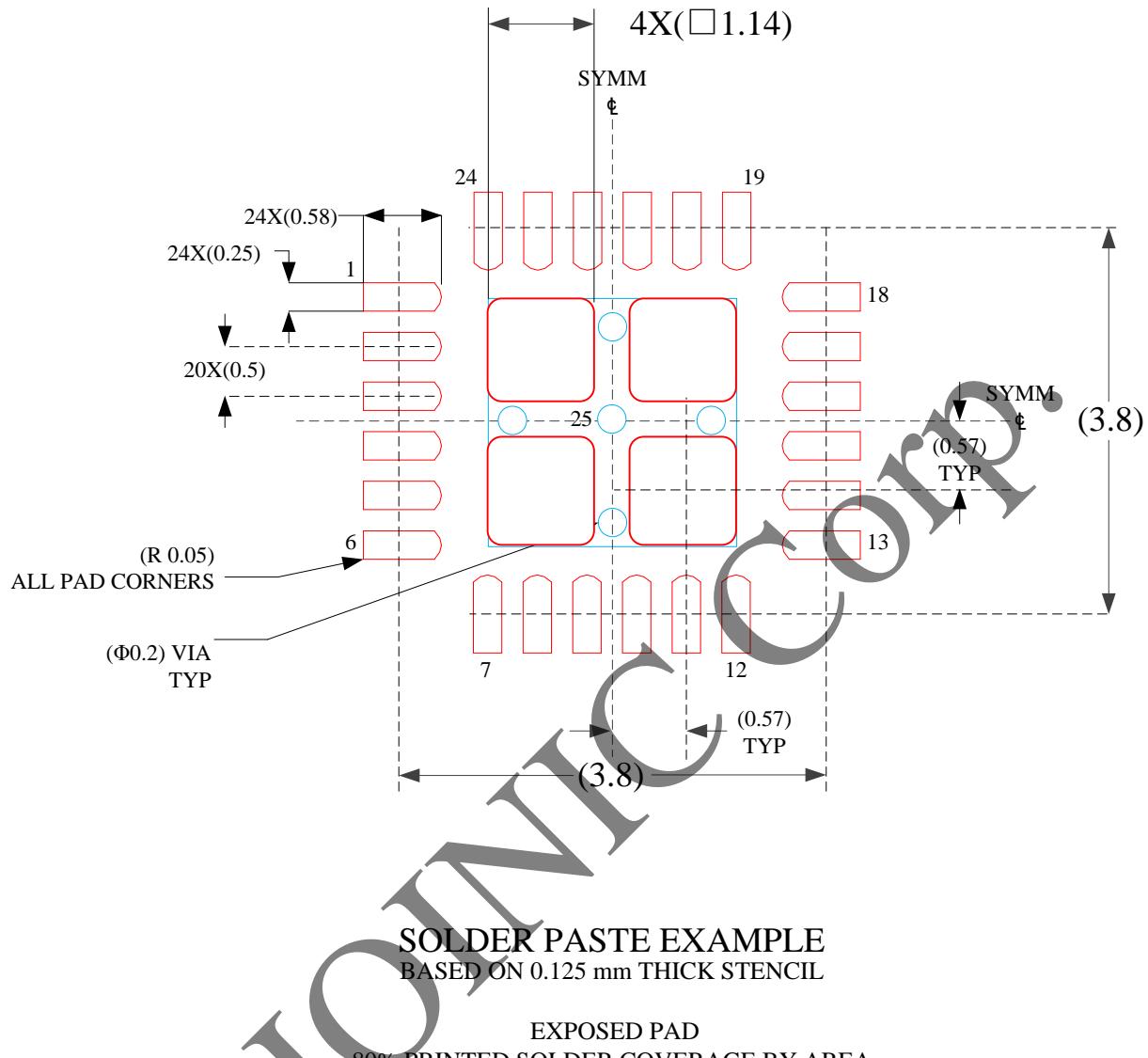
1. The capacitor C2 on VIN should be close to the VIN pin of the IC, so that the loop area can be minimized at these points from VIN to PGND via the capacitor;
2. Capacitor C3 shall be placed close to the LX and BST of the IC;
3. The EPAD of IC pad needs to be windowed and punches plentiful enough overholes to ensure good contact between the EPAD with tin and the PGND of system during production;
4. The output feedback line to the VOUT PIN of chip needs to be far away from the LX line, and ground isolation should be used between the two lines.
5. The current sampling line for 5mohm resistance shall be directly drawn from both ends of the resistance. The line should be parallel, as short as possible and avoid LX and other nodes;
6. The loop composed of RC circuit of LX, LX pin and PGND of IC shall be as small as possible on the PCB board;
7. The GND of the input and output capacitors must be connected to the PGND of a large area;
8. When the program on the USB holder without DP/DM pins, the PCB shall reserve DP/ DM interface, to facilitate the device for subsequent upgrades.
9. The following paths with high currents flowing through them should be thickened:
  - The VIN of the input positive IC shall be copper-lined;
  - the LX of the IC to the inductor L1 shall be copper-lined as short as possible;
  - The output VOUT network shall be copper-lined;

## 17 Package



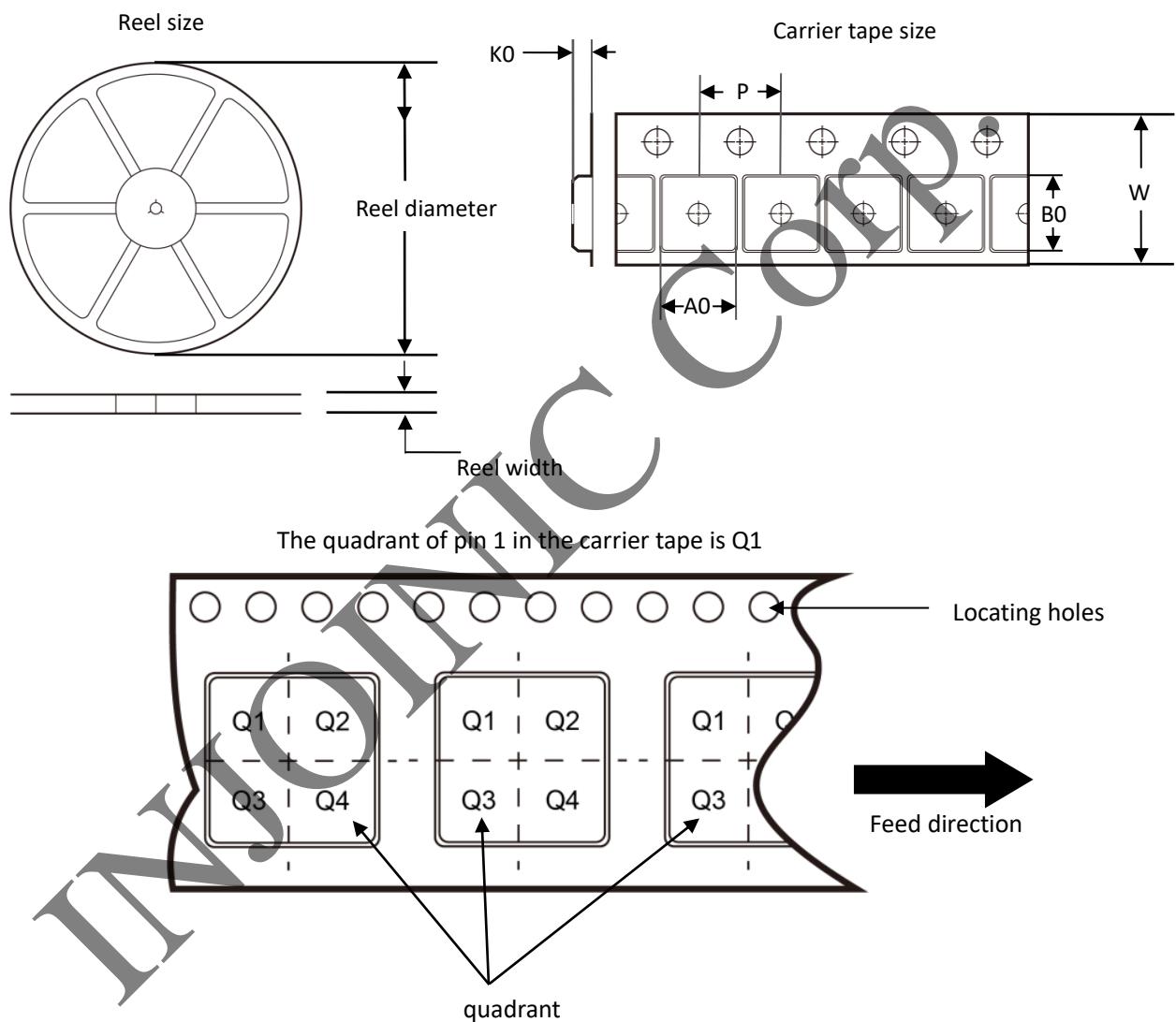
	SYMBOL	MIN	NOM	MAX
Total THICKNESS	A	0.7	0.75	0.8
STAND OFF	A1	0	0.035	0.05
MOLD THICKNESS	A2	--	0.55	--
L/F THICKNESS	A3	0.203 REF		
LEAD WIDTH	b	0.2	0.25	0.3
BODY SIZE (X)	D	4 BSC		
BODY SIZE (Y)	E	4 BSC		
LEAD PITCH	e	0.5 BSC		
EP SIZE (X)	J	2.35	2.45	2.55
EP SIZE (Y)	K	2.35	2.45	2.55
LEAD LENGTH	L	0.35	0.4	0.45
PACKAGE EDGE TOLERANCE	aaa	0.1		
MOLD FLATNESS	bbb	0.1		
COPLANARITY	ccc	0.08		
LEAD OFFSET	ddd	0.1		
EXPOSED PAD OFFSET	eee	0.1		





## 18 Tape and Packaging Information

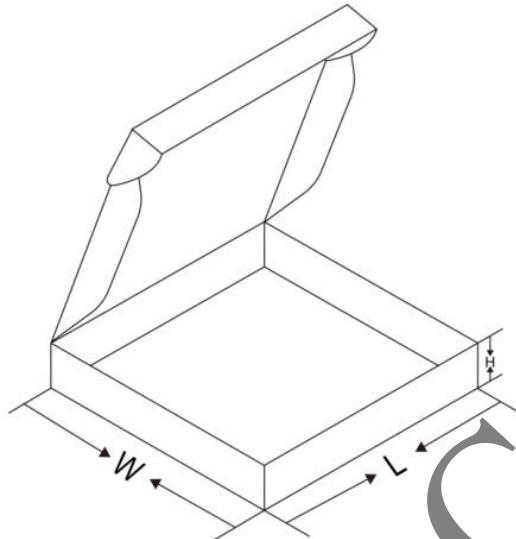
### 18.1 Tape Information



\*All sizes are standard

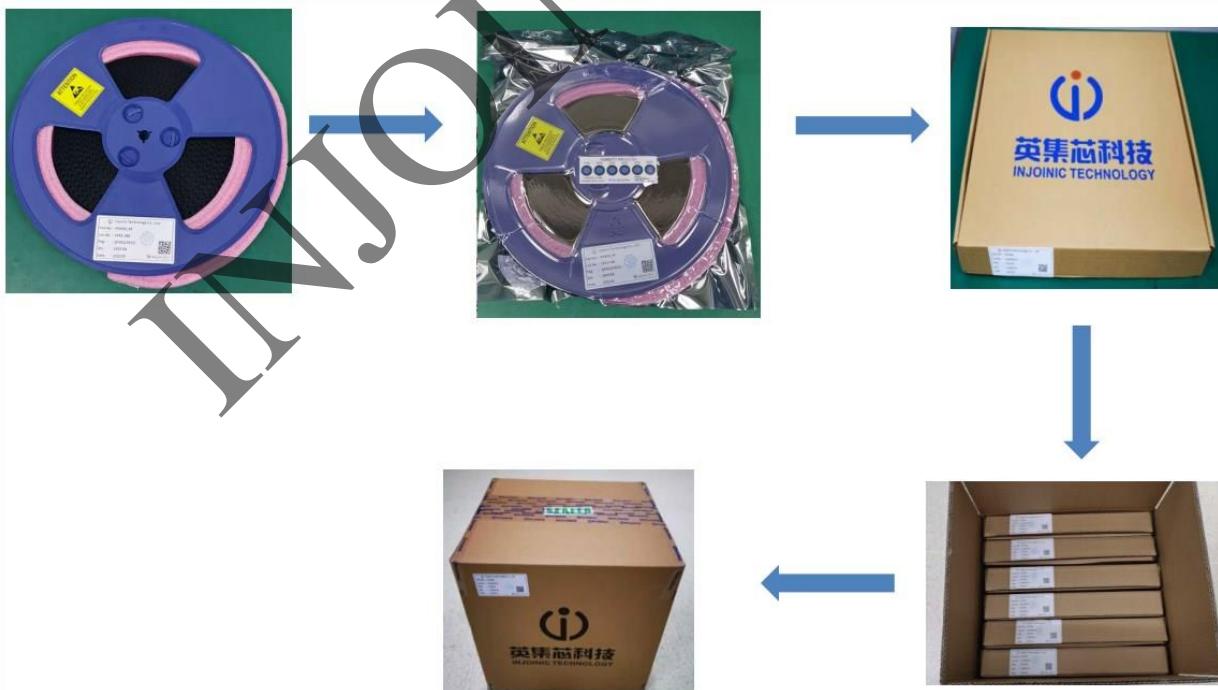
IC model	Pkg	Pin num	standard quantity	Reels diameter (mm)	Reels Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P (mm)	W (mm)	Pin1 quadrant
IP6529_Q1	QFN24	24	5000	330	12.5	4.45 ±0.10	4.50 ±0.10	1.2 ±0.10	8.0 ±0.1	12 ±0.3	Q1

## 18.2 Reel Packaging Carton Specifications



\*All sizes are standard

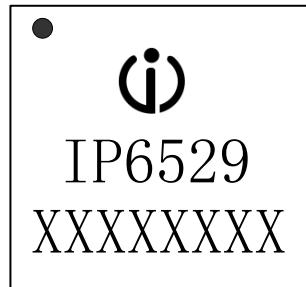
Package form	Packaging method	Only/disc	Disc/inner box	Only/box	Inner box/carton	Only/carton	Inner box length (mm)	Inner box width (mm)	Inner box height (mm)
QFN24	Taping	5000	2	10000	6	60000	360	360	50



Carton size:385\*345\*380mm

Inner box size:360\*360\*50mm

## 19 Silk Screen Information

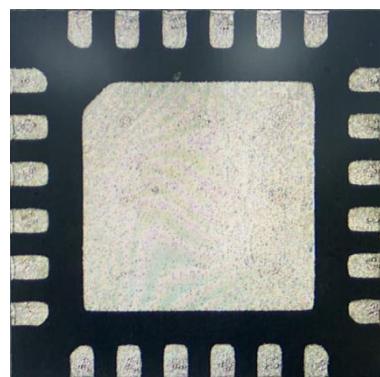


Illustrate:

- 1、 --INJOINIC LOGO
- 2、IP6529 --Product model
- 3、XXXXXXX--Production lot number
- 4、● --PIN1 location identification

IP6529\_Q1 Silk screen instructions

## 20 Photos of Physical Objects



## IMPORTANT NOTICE

INJOINIC TECHNOLOGY and its subsidiaries reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to INJOINIC TECHNOLOGY's terms and conditions of sale supplied at the time of order acknowledgment.

INJOINIC TECHNOLOGY assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using INJOINIC TECHNOLOGY's components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of INJOINIC TECHNOLOGY's components in its applications, notwithstanding any applications-related information or support that may be provided by INJOINIC TECHNOLOGY. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify INJOINIC TECHNOLOGY and its representatives against any damages arising out of the use of any INJOINIC TECHNOLOGY's components in safety-critical applications.

Reproduction of significant portions of INJOINIC TECHNOLOGY's information in INJOINIC TECHNOLOGY's data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. INJOINIC TECHNOLOGY is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

INJOINIC TECHNOLOGY will update this document from time to time. The actual parameters of the product may vary due to different models or other items. This document voids all express and any implied warranties.

Resale of INJOINIC TECHNOLOGY's components or services with statements different from or beyond the parameters stated by INJOINIC TECHNOLOGY for that component or service voids all express and any implied warranties for the associated INJOINIC TECHNOLOGY's component or service and is an unfair and deceptive business practice. INJOINIC TECHNOLOGY is not responsible or liable for any such statements.