# Maximum 36V Input Buck Controller with Dual DCP Protocol

## 1 Features

- **Synchronous-rectified buck converter**
  - ✧ Dual N-channel MOSFET Driver
  - ✧ Input voltage range: 4.5V~36V
  - ✧ Support inductor peak current limiting
  - ✧ Support dual output average current limiting
  - ✧ Support low ESR output capacitors
  - ✧ Support line compensate function
  - ✧ Support CV/CC output mode
- **Charge output protocol**
  - ✧ Support BC1.2, Apple and Samsung
- **Multi-protection and high reliability**
  - ✧ Support input over voltage and under voltage protection
  - ✧ Support output short circuit and over current protection
  - ✧ Over temperature protection
  - ✧ ESD 4KV
  - ✧ DC voltage withstand 48V
- **Package: QFN16(0303)**

## 2 Applications

- **Car Charger**
- **Fast Charge Adaptor**
- **Smart Power Strip**
- **Dash Cam**

## 3 Description

IP6550 integrates a Synchronous-Rectified Buck driver and DCP output standards with dual USB A output ports. It provides solutions for car charger, fast charge adaptor, smart power strip and dash cam.

IP6550 supports up to 36V input voltage, integrated peak inductance current limiting and dual output average current limiting functions.

IP6550 supports FB voltage regulation mode, output voltage can be adjusted to the needs of the system by means of a peripheral circuit.

IP6550 output has CV/CC mode, when the output current is lower than preset value, the output voltage will be constant in CV output mode; when the output current is higher than preset value, the output voltage will decrease in CC output mode.

IP6550 supports output line compensation, when output current increases, the output voltage will increase accordingly that makes up the resistive voltage drop introduced by connection, wire, and PCB traces.

IP6550 supports soft start function that protects the input power from inrush current at start up.

IP6550 supports multi-protection on input overvoltage and under voltage, output over current, overvoltage, under voltage and short circuit.

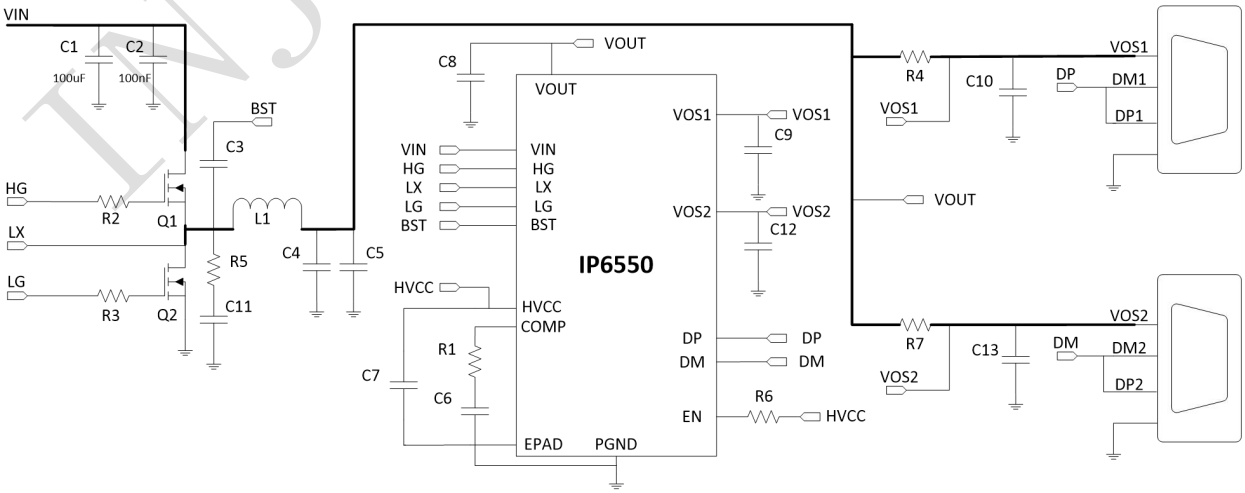



**Figure 1. IP6550 dual USB A output ports simplified application schematic diagram**



## 4 Pin Functions

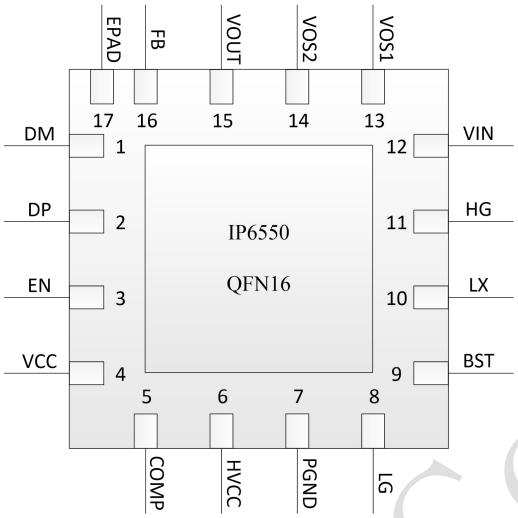



**Figure 2. Pin functions**

| Pins | | Description |
|---|---|---|
| Pin No. | Pin Name | |
| 1 | DM | Connect to USB DM data line |
| 2 | DP | Connect to USB DP data line |
| 3 | EN | DCDC enable pin |
| 4 | VCC | VCC LDO pin |
| 5 | COMP | Control loop compensating pin |
| 6 | HVCC | Power output pin for driver LDO |
| 7 | PGND | Power ground |
| 8 | LG | Low voltage side NMOS gate drive pin |
| 9 | BST | Connect to bootstrap capacitor |
| 10 | LX | DCDC switch point, connect to inductor |
| 11 | HG | High voltage side NMOS gate drive pin |
| 12 | VIN | Power input |
| 13 | VOS1 | VOUT1 output current negative sense pin |
| 14 | VOS2 | VOUT2 output current negative sense pin |
| 15 | VOUT | Output voltage sense pin/output current positive sense pin |
| 16 | FB | External feedback pin |
| 17 | EPAD | Ground |



## 5 IP6550 Series Product Introduction

| Product | Introduction |
|---|---|
| IP6550_DUAL_4A8 | Single port output 5V/2.4A, dual ports output 5V/4.8A with Dual DCP Protocol; |
| IP6550_FB | IP6550 output voltage is controlled through FB.<br>Maximum output current is 5A(5mohm sensing resistor); |
| IP6550_IIC | IP6550 output power is controlled by IIC; |



## 6 Absolute Maximum Ratings

| Parameters | Symbol | Value | Unit |
|---|---|---|---|
| Input voltage | $V_{IN}$ | -0.3 ~ 48 | **V** |
| LX voltage | $V_{LX}$ | -0.3 ~ VIN+0.3 | **V** |
| BST voltage | $V_{BST}$ | -0.3 ~ 54 | **V** |
| VOUT voltage | $V_{VOUT}$ | -0.3 ~ 30 | **V** |
| DM/DP voltage | $V_{DM/DP}$ | -0.3 ~ 6 | **V** |
| Junction temperature | $T_J$ | -40 ~ 150 | ℃ |
| Storage temperature | Tstg | -60 ~ 150 | ℃ |
| Ambient Temperature | $T_A$ | -40~120 | ℃ |
| Thermal resistance (junction to ambient) | $\theta_{JA}$ | 50 | **℃/W** |
| Human body model (HBM) | ESD | 4 | **KV** |

*Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to Absolute Maximum Rated conditions for extended periods may affect device reliability.

## 7 Recommended Operating Conditions

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Input voltage | $V_{IN}$ | 4.5 | | 36 | V |

*Device's performance cannot be guaranteed when working beyond those Recommended Operating Conditions.



## 8 Electrical Characteristics

Unless otherwise specified, the test IC is IP6550_Dual_4A8,TA =25℃, L=22uH, VIN=12V, VOUT=5V

| Parameters | Symbol | Test Condition | Min. | Typ. | Max | Unit |
|---|---|---|---|---|---|---|
| **Input system** | | | | | | |
| Input voltage | $V_{IN}$ | | 4.5 | | 36 | V |
| Input under voltage | $V_{IN-UV}$ | Rising voltage | 4.3 | 4.5 | 4.65 | V |
| | $V_{IN-UV-TH}$ | Hysteresis voltage | | 0.4 | | V |
| Input over voltage | $V_{IN-OV}$ | Rising voltage | 35 | 36 | 38 | V |
| | $V_{IN-OV-TH}$ | Hysteresis voltage | | 0.8 | | V |
| Input quiescent current | $I_Q$ | VIN=12V, VOUT=5V@0A, no switching | | 0.4 | 0.7 | mA |
| Shutdown current | $I_{SD}$ | VIN=12V，EN=0V | | 0.3 | | mA |
| **Drive system** | | | | | | |
| HG pull-up resistor | $R_{HG\_PU}$ | | | 3 | | Ω |
| HG pull-down resistor | $R_{HG\_PD}$ | | | 3 | | Ω |
| LG pull-up resistor | $R_{LG\_PU}$ | | | 3 | | Ω |
| LG pull-down resistor | $R_{LG\_PD}$ | | | 3 | | Ω |
| Dead time | $T_{Dead}$ | VIN=12V，VOUT=5V | | 40 | | ns |
| HG maximum duty cycle | $D_{HG\_MAX}$ | VIN=12V，FS=135kHz | | 97.5 | | % |
| Switching frequency | $F_S$ | VIN=12V，VOUT=5V | 135 | 145 | 155 | kHz |
| **Output system** | | | | | | |
| Output voltage | $V_{OUT}$ | Voltage Feedback through VOUT PIN | 3 | | 20 | V |
| Output voltage ripple | $\Delta V_{OUT}$ | VIN=24V，VOUT=5V@3A Cout: 100uf solid-state cap | 70 | 80 | 90 | mV |
| Soft start time | $T_{SS}$ | VIN=12V，VOUT=5V | | 3 | | ms |
| Output line compensate voltage | $V_{COMP}$ | VIN=12V，VOUT=5V，IOUT=1A | | 40 | | mV |
| Output current in CC mode | $I_{OUT}$ | IP6550_DUAL_4A8 Single port output | | 2.4 | | A |
| | | IP6550_DUAL_4A8 Dual ports output | | 4.8 | | A |
| Output overvoltage threshold | $V_{OUT}$ | After the output enters CC mode, the output hiccup restart voltage | | 2.9 | | V |



| | | | | | | |
|---|---|---|---|---|---|---|
| Thermal shutdown temperature | $T_{OTP}$ | Rising temperature | | 150 | | ℃ |
| Thermal shutdown temperature hysteresis | $\Delta T_{OTP}$ | | | 110 | | ℃ |
| **VCC LDO OUTPUT** | | | | | | |
| VCC LDO output voltage | VCC | | | 3.3 | | V |
| VCC LDO output power | $I_{VCC}$ | | | | 20 | mA |
| **EN PIN** | | | | | | |
| EN PIN turn-on voltage | $V_{EN-ON}$ | | | 2.0 | | V |
| EN PIN hysteresis voltage | $V_{EN-TH}$ | | | 0.2 | | V |
| EN PIN turn-on delay | $T_{EN-ON}$ | | | 800 | | us |
| EN PIN turn-off delay | $T_{EN-OFF}$ | | | 100 | | us |



# 9 Function Description

## Internal Block Diagram

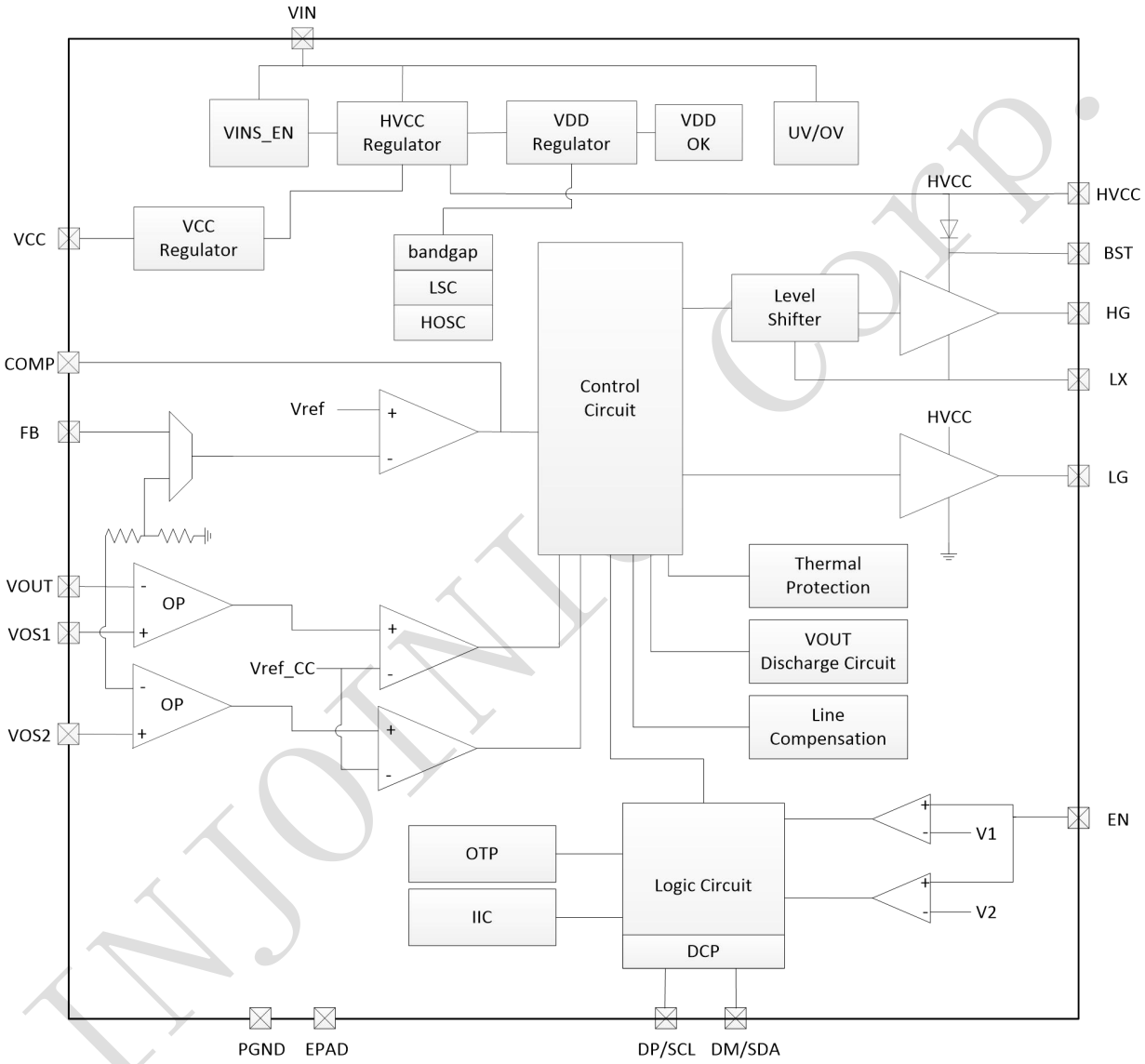



**Figure3 IP6550 Internal block diagram**

## Synchronized Switch Buck Driver

IP6550 integrates a synchronized switch buck driver, input voltage ranges from 4.5V to 36V and output from 3.0V to 20V.

IP6550 integrates peak inductance current limiting and dual output average current limiting

functions.

IP6550 output is driven at a switching frequency of 135kHz, It can be adjusted internally.

IP6550 has soft start function, preventing the huge inrush current cause damage to the IC. When VIN=24V, VOUT=5V, the soft start time is 3ms.

The MOSFET $R_{DS(ON)}$ = 5.5mohm@$V_{GS} = 10V$ When VIN=24V, VOUT=5V@5A, the conversion efficiency is 95%.

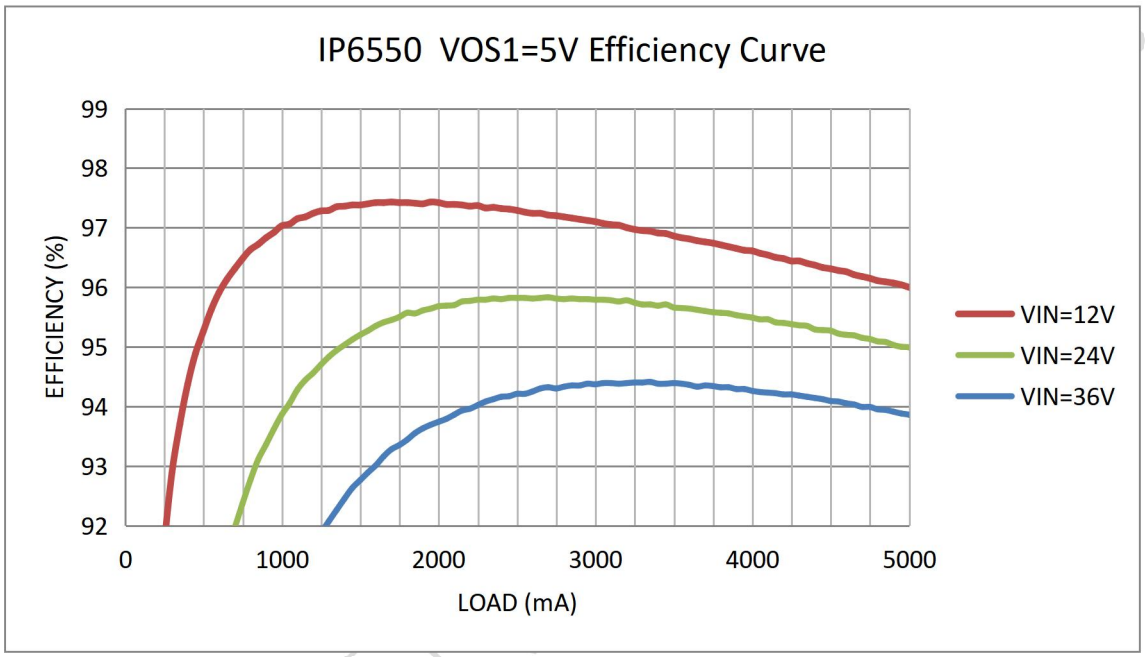



**Figure 4. IP6550 VOS1 output efficiency curve**

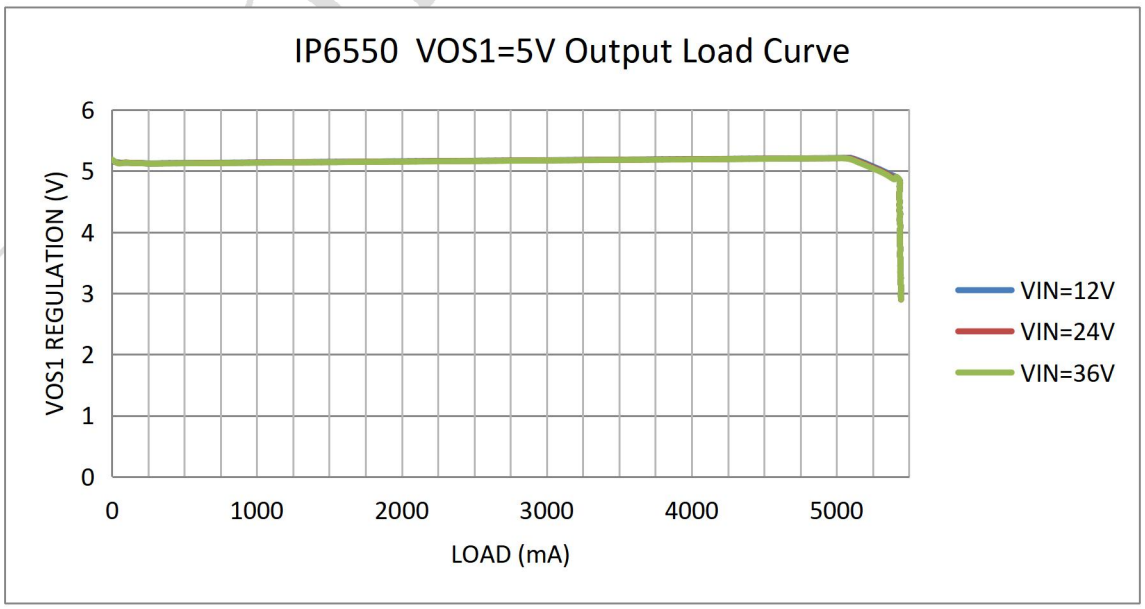



**Figure 5. IP6550 VOS1-IOUT curve**

## Output Voltage Line Compensate

IP6550 supports output line compensate, output voltage will increase about 40mV as output current increase 1A.

## Output CV/CC Characteristic

IP6550 output has CV/CC mode: when the output current is lower than preset value, the output is in CV mode with constant voltage; when the output current is higher than preset value, the output is in CC mode with decreasing output voltage. The load current continues to increase and the output voltage rapidly decreases until the output voltage undervoltage protection is triggered.

## Output CC Current Set

IP6550 VOUT1 output current limit can be adjusted by regulate the 5mOhm sensing resistor between VOUT and VOS1. VOUT2 output current limit can be adjusted by regulate the 5mOhm sensing resistor between VOUT and VOS2. The load current is measured by detect the voltage drop between VOUT and VOS.

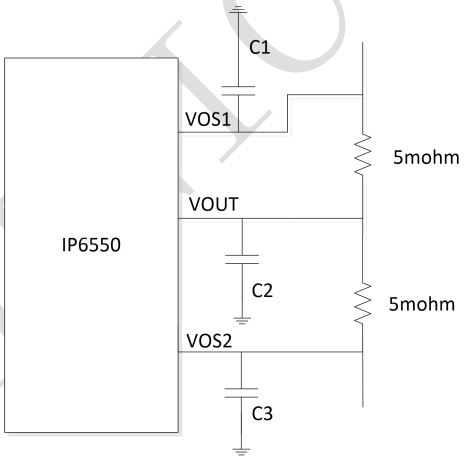



**Figure 6. IP6550 dual output current limiting circuit**

When the value of 5mohm current detect resistor is changed, the current limit of VOUT1 and VOUT2 will change accordingly.

In PCB layout, pay attention to the trace routing of VOS1/VOS2 and VOUT, the trace should go out directly from the two side of 5mOhm resistor, avoiding introduce current limit deviation because of additional PCB trace resistor. Other than that, the 10mOhm resistor should use alloy resistor with good temperature coefficient (100ppm) and high precision of 1%.



## Protection Function

IP6550 will detect the VIN voltage, if VIN voltage is lower than 4.5V, IP6550 will enter standby mode and shut down the output.

IP6550 supports input over voltage protection: when the VIN voltage is higher than 36V, IP6550 determines the VIN is over voltage and shutdown the output; when VIN decrease under 35.6V, IP6550 determines the input voltage recovers and opens the output.

IP6550 supports output under voltage protection: if the VOUT voltage is lower than 2.9V, IP6550 determines the output is under voltage and will shut down the output and hiccup restart after 2sec.

IP6550 supports short circuit protect, 16ms after the circuit is started, if VOUT voltage is under 2.9V, IP6550 determines the output is short circuit and will shut down the output and hiccup restart after 2sec.

IP6550 supports over temperature protection: when the temperature detected is higher than 150℃, the output will be shut down. When the temperature decreases below 110℃, IP6550 determines the temperature has recovered and will restart the output.

## Dual Output Ports

IP6550 supports two USB A output ports, single port output power is 5V/2.4A.

When dual ports have attached device, dual ports overall output power is 5V/4.8A and single port output power is 5V/2.4A.

## VCC LDO OUTPUT

The IP6550 integrates a 3.3V output VCC LDO, which maximum carrying capacity is 20mA;

## EN PIN Function

IP6550 supports EN PIN to control the device on and off. There is no internal pull up or down of the EN PIN, and the voltage needs to be controlled by external control.

When the device detects that the EN PIN voltage is greater than the upper EN input threshold, the DCDC function is enabled. When the device detects that the EN PIN voltage is lower than the lower EN input threshold, turn off the DCDC.

## IIC/FB Control

The IP6550 supports IIC control. As Salve, the external device can control output voltage and CC limit value by IIC.

IP6550 supports FB external feedback. For the devices that support FB external feedback, the FB voltage is 0.84V.



# 10 Application Notes

## Input Capacitance Selection

The ESR of the input capacitor should be as small as possible. The ESR will affect the conversion efficiency of the system.

The maximum ripple current supported by the input capacitor must be greater than the maximum VIN ripple current of the system. The ripple current RMS value of the input capacitor is calculated as follows:

$$I_{RMS} = I_{LOAD} * \sqrt{\frac{V_{OUT}}{V_{IN}} * (1 - \frac{V_{OUT}}{V_{IN}})}$$

$I_{LOAD}$ is the load current, $V_{IN}$ is the input voltage, $V_{OUT}$ is the output voltage.

## Inductance Selection

The inductor with 22uH is recommended for most applications.

The DCR of inductor has great influence on the conversion efficiency of the system, low DCR inductors are recommended. For solutions above 30W, it is recommended to use an inductor with a DCR of less than 10mohm.

The inductor saturation current should be at least 20% greater than the system's peak inductor current limit, In order to avoid inductance saturation, resulting in a decrease in inductance, system instability.

The calculation formula of the PEAK current ($I_{L(PEAK)}$) is as follows:

$$I_{L(PEAK)} = I_{LOAD} + \frac{\Delta I_L}{2}$$

$I_{LOAD}$ is the LOAD current, $\Delta I_L$ is the peak-to-peak value of the inductor current, The calculation formula of $\Delta I_L$ is as follows:

$$\Delta I_L = \frac{V_{OUT} * (V_{IN} - V_{OUT})}{V_{IN} * L * F_S}$$

$V_{IN}$ is the input voltage, $V_{OUT}$ is the output voltage, L is the inductance, $F_S$ is the switching frequency;

## Output Capacitance Selection

The output capacitance is used to keep the output stable. The value of ESR and capacitance has an effect on the output ripple. The output ripple voltage $V_{out-ripple}$ can be calculated as follows:

$$V_{out-ripple} = \Delta I_L * (R_{ESR} + \frac{1}{8 * F_S * C_{OUT}})$$

$\Delta I_L$ is the peak-to-peak value of the inductor current, $R_{ESR}$ is the equivalent serial resistance value of the output capacitance, $F_S$ is the switching frequency, $C_{OUT}$ is the output capacitance value.



## MOSFET Selection

It is recommended to choose a $V_{(BR)DSS}$ MOSFET device with at least 20% higher than the input voltage.

$R_{DS(ON)}$ of MOSFET leads to the power loss of the on-device, which has a direct impact ON the conversion efficiency of the system. Generally, it is recommended to choose a 10mohm MOSFET with $R_{DS(ON)}$.

If the solution requires higher power output, lower $R_{DS(ON)}$ devices are recommended.

The $C_{ISS}$ of MOSFET affects its switching speed. It is necessary to adjust the resistance of HG and LG in series according to different MOSFET, and adjust the driving speed of MOSFET to ensure the system stability.

It are advised to choose the MOSFET which $C_{ISS}$ value is less than 1000pF.

The RC buffer circuit of LX can suppress the burr of LX. The proper RC buffer circuit can make the system have better EMI effect.

For the circuit of the driving part, it is recommended to reserve HG and LG series resistors of 0603 specifications and RC buffer circuit as shown in the following figure.

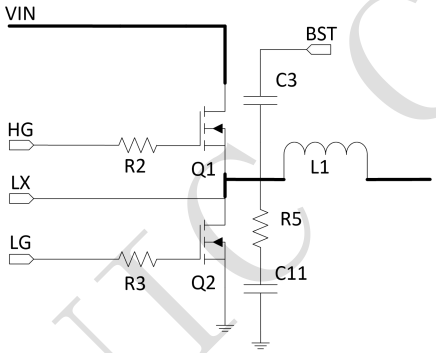



**Figure 7. IP6550 MOSFET drive circuit diagram**

## FB Feedback

IP6550 supports the function of FB external feedback. For the devices that support FB voltage regulating, the FB voltage is 0.84V. The circuit is as follows:

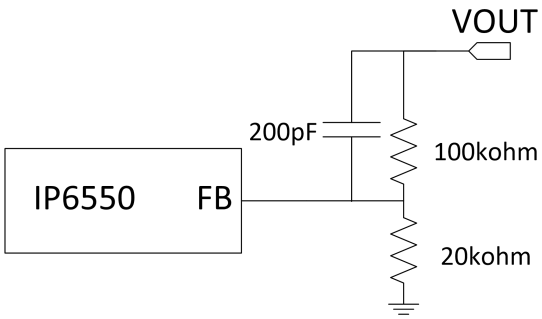



**Figure 8. IP6550 FB feedback circuit diagram**

The feedback resistance can be adjusted according to the need to get the appropriate output voltage.



## 11 Typical Application Schematic

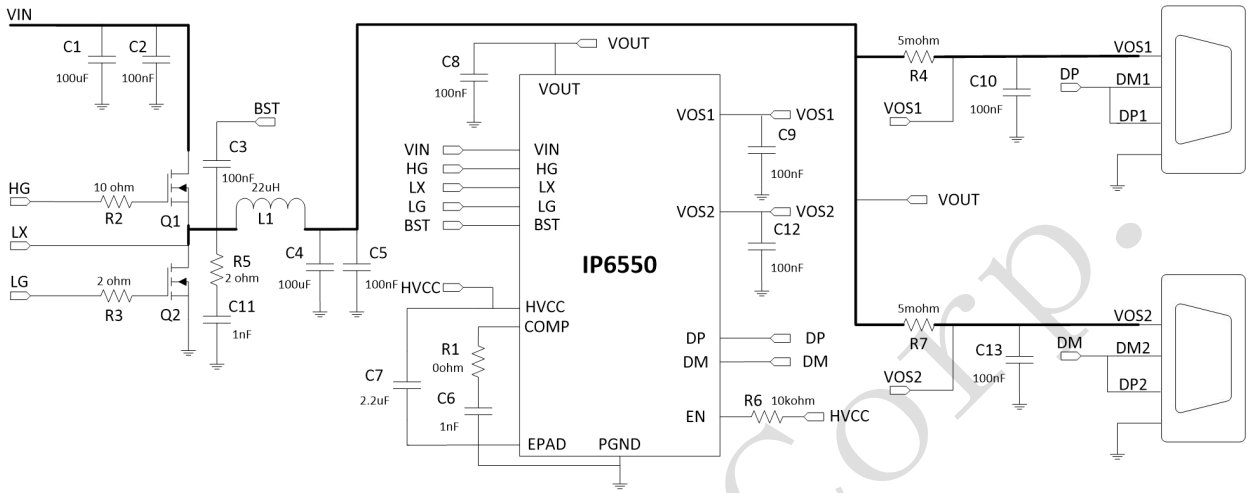



**Figure 9. IP6550 dual USB A output ports application schematic diagram**

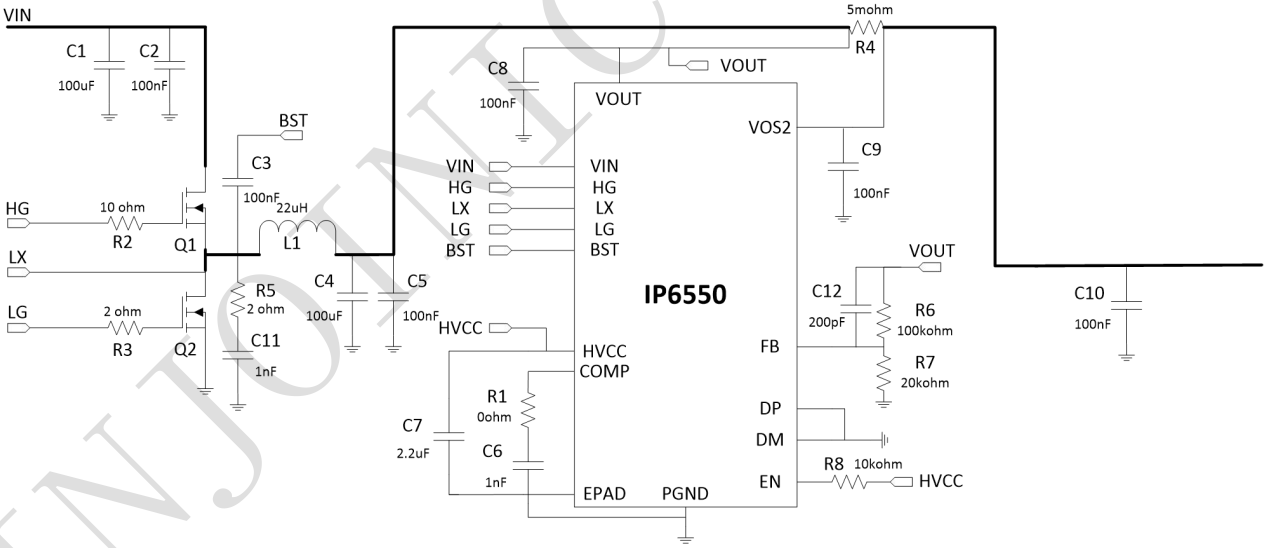



**Figure 10. IP6550_FB external feedback single-port output application schematic diagram**

**NOTES:**

1. In the scheme of achieving VOS2 voltage control by pulling or pouring current in FB, A 2kohm resistor needs to be connected in series between the FB pin of the control device and the FB pin of IP6550_FB.
2. IP6550_FB limits the output current through a 5mohm sensing resistor between VOUT and VOS2.
3. IP6550_FB has enabled the function of EN PIN to control DCDC turn on or off. EN PIN can be connected to HVCC via a 10k resistor if this function is not needed.



## 12 BOM List

With the application of IP6550_DUAL_4A8 dual-port output, the finished BOM is as follows:

| No. | Part Name | Type | Unit | Qty | Location | Notes |
|---|---|---|---|---|---|---|
| 1 | IC | IP6550_DUAL_4A8 | PCS | 1 | | |
| 2 | Inductor | 22uH+/-20%, current 8A DCR<10mohm | PCS | 1 | L1 | |
| 3 | Electrolytic capacitor | 100uF | PCS | 1 | C1 | Withstand voltage higher than 36V |
| 4 | Solid-state capacitor | 100uF | PCS | 1 | C4 | Withstand voltage higher than 6.3V |
| 5 | SMD capacitor | 0603 100nF 10% | PCS | 1 | C2 | Withstand voltage higher than 36V |
| 6 | SMD capacitor | 0603 100nF 10% | PCS | 1 | C3 | Withstand voltage higher than 16V |
| 7 | SMD capacitor | 0603 100nF 10% | PCS | 6 | C5、C8、C9、C10、C12、C13 | Withstand voltage higher than 6.3V |
| 8 | SMD capacitor | 0603 1nF 10% | PCS | 2 | C6、C11 | Withstand voltage higher than 36V |
| 9 | SMD capacitor | 0603 2.2uF 10% | PCS | 1 | C7 | Withstand voltage higher than 16V |
| 10 | SMD resistor | 0603 0R 5% | PCS | 1 | R1 | |
| 11 | SMD resistor | 0603 20R 5% | PCS | 1 | R2 | |
| 12 | SMD resistor | 0603 2R 5% | PCS | 2 | R3、R5 | |
| 13 | SMD resistor | 0603 10k ohm 5% | PCS | 1 | R6 | |
| 14 | SMD resistor | 1206 5mohm 1% precision, temperature coefficient less than 100ppm | PCS | 2 | R4、R7 | Current sense resistor |
| 15 | MOSFET | MOSFET | PCS | 2 | Q1、Q2 | |



## 13 Considerations for PCB layout

IP6550 integrates step-down controller. PCB layout is important for system stability, EMI, and other performance indicators. The PCB layout suggestions are as follows:

1. The loop composed of input capacitor and upper tube NMOS and lower tube NMOS should be as small as possible;

2. The inductor cable connecting the upper pipe and the lower pipe should be as wide and short as possible, so that the node area can ensure the maximum output current capacity;

3. The loop composed of LX buffer circuit and PGND should be as small as possible;

4. The current sampling line for 5Mohm resistance is directly drawn from both ends of the resistance. The line is parallel, as short as possible and avoids SW and other nodes;

5. The capacitance of HVCC and COMP is placed close to the device PIN;

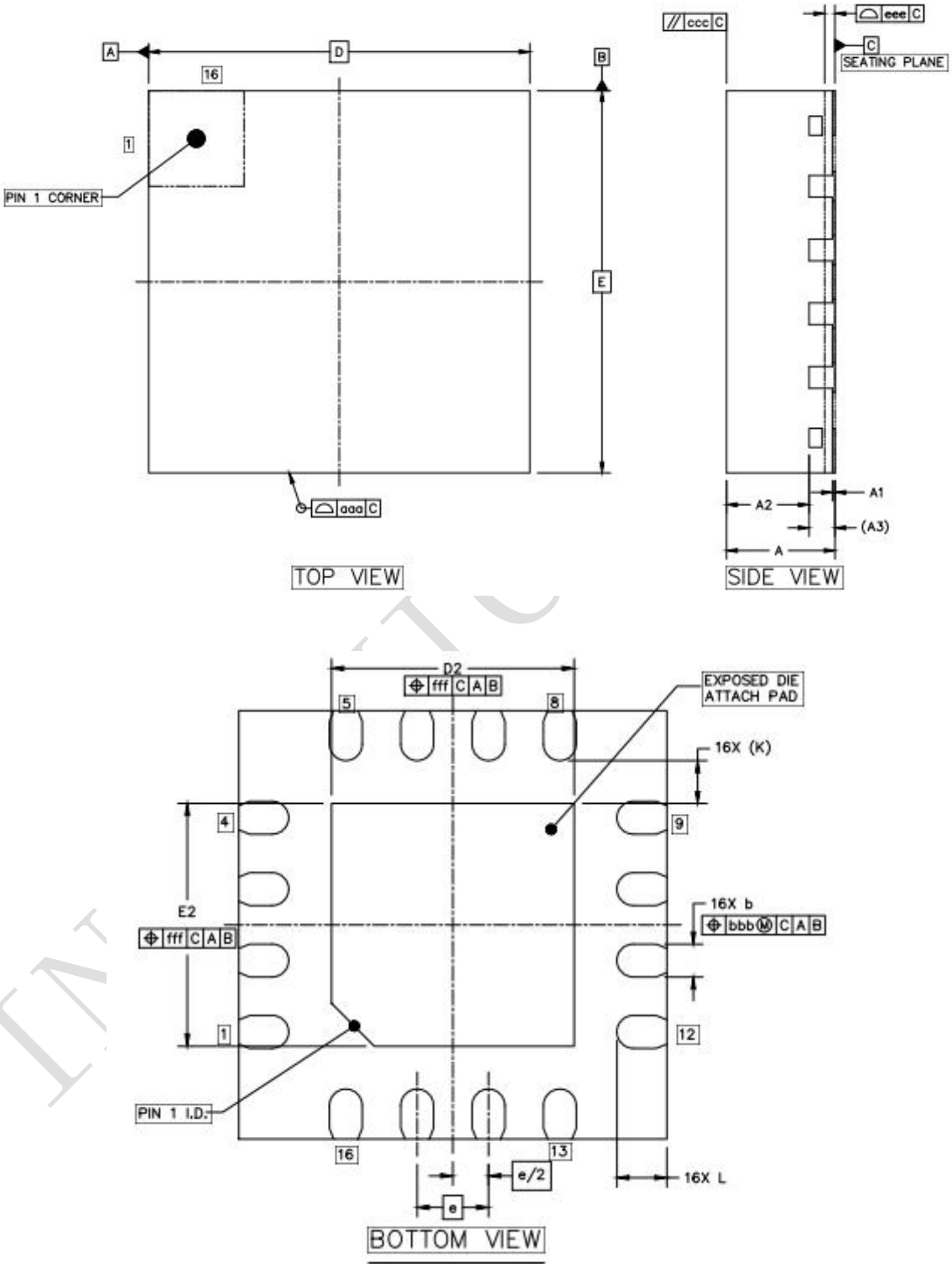
6. The GND of the input and output capacitors must be connected to the PGND of a large area;

7. Please refer to the IP6550 Application Notes for further information.

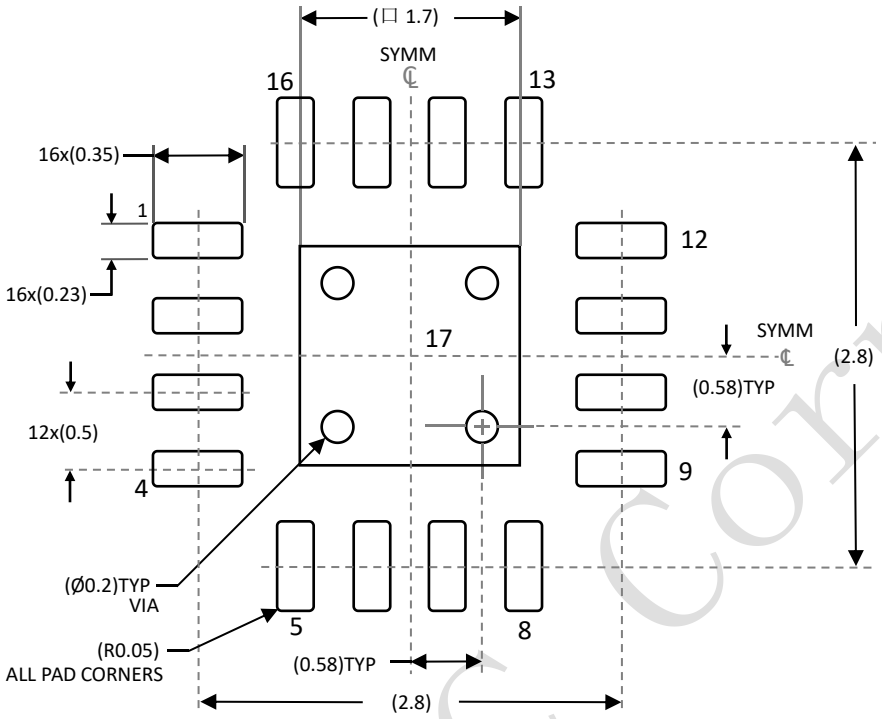


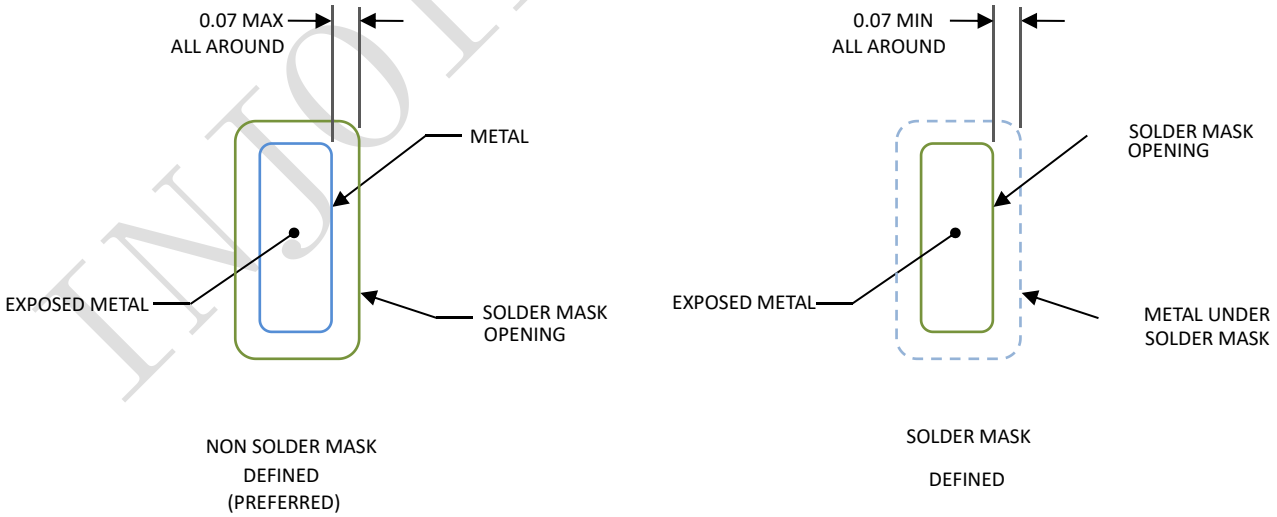
 

## 14 Package

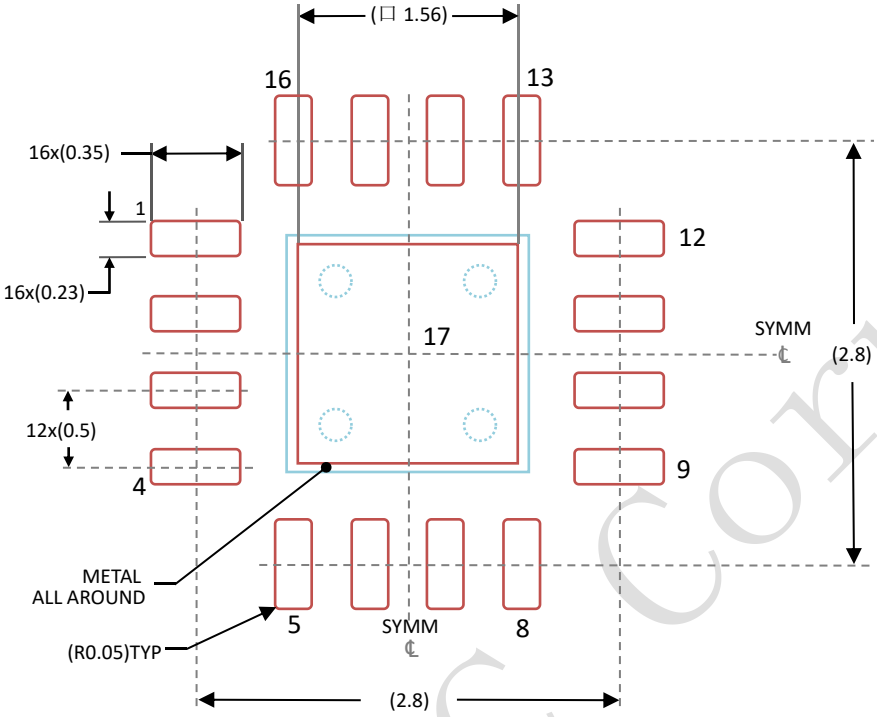


| | SYMBOL | MIN | NOM | MAX |
|---|---|---|---|---|
| Total THICKNESS | A | 0.7 | 0.75 | 0.8 |
| STAND OFF | A1 | 0 | 0.02 | 0.05 |
| MOLD THICKNESS | A2 | -- | 0.65 | -- |
| L/F THICKNESS | A3 | | 0.203 REF | |
| LESD WIDTH | b | 0.18 | 0.23 | 0.28 |
| BODY SIZE (X) | D | | 3 BSC | |
| BODY SIZE (Y) | E | | 3 BSC | |
| LEAD PITCH | e | | 0.5 BSC | |
| EP SIZE (X) | D2 | 1.6 | 1.7 | 1.8 |
| EP SIZE (Y) | E2 | 1.6 | 1.7 | 1.8 |
| LEAD LENGTH | L | 0.25 | 0.35 | 0.45 |
| LEAD TIP TO EXPOSED PAD EDGE | K | | 0.3 REF | |
| PACKAGE EDGE TOLERANCE | aaa | | 0.1 | |
| MOLD FLATNESS | ccc | | 0.1 | |
| COPLANARITY | eee | | 0.08 | |
| LEAD OFFSET | bbb | | 0.1 | |
| EXPOSED PAD OFFSET | fff | | 0.1 | |



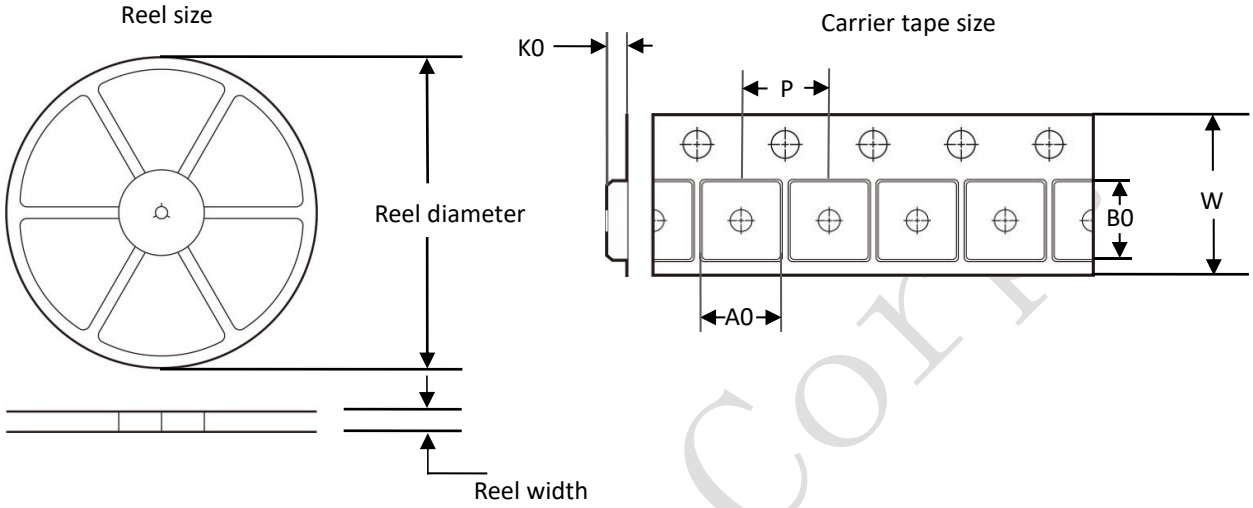



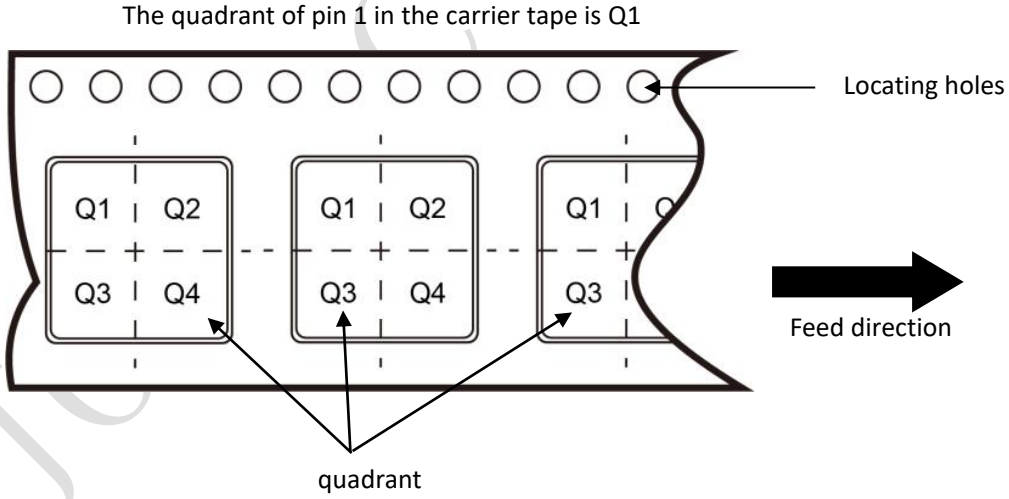

SOLDER MASK DETAILS




SOLDER PASTE EXAMPLE
BASED ON 0.125mm THICK STENCIL
EXPOSED PAD 17:
86% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

## 15 Tape information

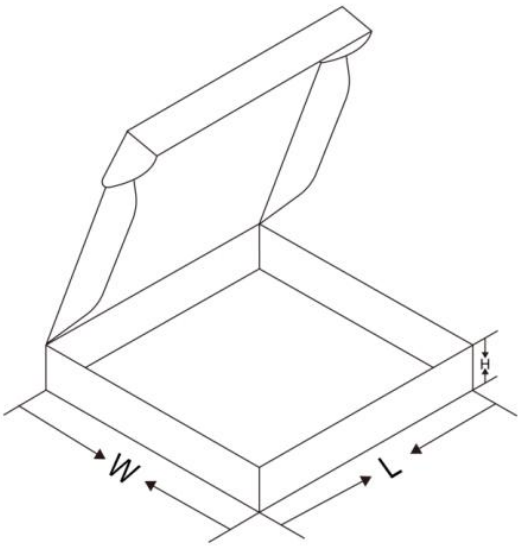



*All sizes are standard

| IC model | Pkg | Pin num | standard quantity | Reels diameter (mm) | Reels Width (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P (mm) | W (mm) | Pin1 quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|
| IP6550 | QFN16 | 16 | 5000 | 330 | 12.5 | 3.30 ±0.10 | 3.30 ±0.10 | 1.05 ±0.10 | 4.00 ±0.1 | 12 ±0.3 | Q1 |

Reel packaging carton specifications



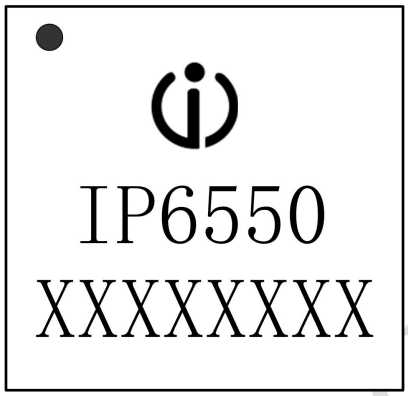

*All sizes are standard

| Package form | Packaging method | Only/disc | Disc/inner box | Only/box | Inner box/carton | Only/carton | Inner box length（mm） | Inner box width（mm） | Inner box height（mm） |
|---|---|---|---|---|---|---|---|---|---|
| QFN16 | Taping | 5000 | 2 | 10000 | 6 | 60000 | 360 | 360 | 50 |


**Carton size:385*345*380mm**

**Inner box size:360*360*50mm**

## 16 Silk screen information

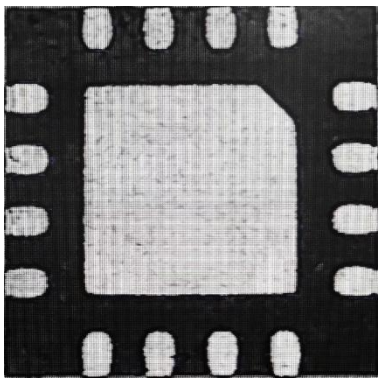



Illustrate:

1、 --INJOINIC LOGO
2、IP6550 --Product model
3、XXXX --Production lot number
4、● --PIN1 location identification

IP6550 Silk screen instructions

## 17 Photos of physical objects

# IMPORTANT NOTICE

INJOINIC TECHNOLOGY and its subsidiaries reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to INJOINIC TECHNOLOGY's terms and conditions of sale supplied at the time of order acknowledgment.

INJOINIC TECHNOLOGY assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using INJOINIC TECHNOLOGY's components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of INJOINIC TECHNOLOGY's components in its applications, notwithstanding any applications-related information or support that may be provided by INJOINIC TECHNOLOGY. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify INJOINIC TECHNOLOGY and its representatives against any damages arising out of the use of any INJOINIC TECHNOLOGY's components in safety-critical applications.

Reproduction of significant portions of INJOINIC TECHNOLOGY's information in INJOINIC TECHNOLOGY's data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. INJOINIC TECHNOLOGY is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

INJOINIC TECHNOLOGY will update this document from time to time. The actual parameters of the product may vary due to different models or other items. This document voids all express and any implied warranties.

Resale of INJOINIC TECHNOLOGY's components or services with statements different from or beyond the parameters stated by INJOINIC TECHNOLOGY for that component or service voids all express and any implied warranties for the associated INJOINIC TECHNOLOGY's component or service and is an unfair and deceptive business practice. INJOINIC TECHNOLOGY is not responsible or liable for any such statements.

