2-Series to 4-Series Lithium-ion Secondary Protection Chip with External Delay Capacitor

1 Features

- **2-series, 3-series, and 4-series cell overvoltage protection**
- **External capacitor-programmed delay timer**
- **Overcharge protection voltage V_{OV}: 3.85V~4.60V(Step:10mV)**
- **Overcharge protection voltage hysteresis: (Step:50mV)**
  0~300mV(3.85V≤V_{OV}<4.00V)
  0~500mV(4.00V≤V_{OV}≤4.60V)
- **Accuracy of overcharge protection voltage (V_{OV}): ±20mV**
- **Quiescent current: 1μA@25°C**
- **Low leakage current per cell input < 100nA**
- **Output drive: active high**
- **High 30V absolute maximum rating**
- **Package: DFN8(0202)**

2 Applications

- **Laptop**
- **Uninterruptible power supply (UPS) backup battery**

3 Overview

The IP3247 is an overvoltage monitor and protector for 2 to 4 series Li-Ion battery pack systems. Each cell is monitored independently for an overvoltage condition.

When the IP3247 detects an overvoltage condition on any cell, the delay time is set by the free discharge time of the external capacitor on the CD pin . When the time delay expires, the overvoltage protection will be driven. If the CD pin is open or short circuited, it shall be timed according to the internal fixed time. When the overvoltage time meets the delay time, the overvoltage protection will be driven.

In order to achieve faster production-line testing, the IP3247 devices provide a customer test mode with a shorter delay time.

The IP3247 provides DFN8 (0202) package.

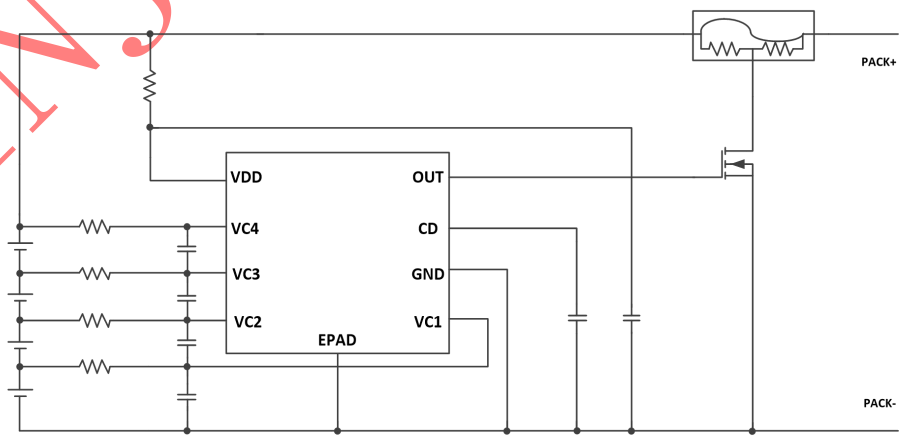


Figure 1: IP3247 Simplified Application Circuit

4 Pin Configuration and Functions

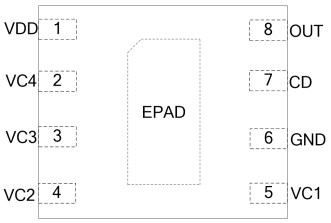


Figure 2: IP3247 DFN8(0202) Pin Functions

Pin	Name	Description
1	VDD	The power pin of the chip, connected to RC for filtering.
2	VC4	Positive terminal of cell 4. RC is connected between the positive and the negative terminal of cell 4 for filtering.
3	VC3	Negative terminal of cell 4, positive terminal of cell 3, RC is connected between them for filtering.
4	VC2	Negative terminal of cell 3, positive terminal of cell 2, RC is connected between them for filtering.
5	VC1	Negative terminal of cell 2, positive terminal of cell 1, RC is connected between them for filtering.
6	GND	The ground pin of the chip, negative terminal of cell 1.
7	CD	The overvoltage delay setting pin, connected to the capacitor to the ground. The capacitor is set according to the delay. If the CD pin is open or short circuited, the delay is a fixed delay set internally.
8	OUT	Output port, output high-level drive protection.
	EPAD	Thermal pad, recommended to connect to GND.

5 Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
High Voltage Pin Input Range	VDD,VC4,VC3,VC2,VC1,OUT	-0.3 ~ 30	V
High Voltage Pin Input Range	CD	-0.3 ~ 30	V
Storage Temperature Range	Tstg	-60 ~ 150	°C
Thermal Resistor (Junction to Ambient)	θ_{JA}	120	°C/W
ESD (Human Body Model)	ESD	4	KV

*Stresses beyond these listed parameters may cause permanent damage to the device.

Exposure to Absolute Maximum Rated conditions for extended periods may affect device reliability.

6 Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input Voltage	VDD	6	--	20	V
Operating Temperature	T_A	-40	--	110	°C

*Device performance cannot be guaranteed when working beyond these recommended operating conditions.

7 Configuration Selection Table

IP3247 XX

IC CODE
Range: from AA to ZZ

Table 1: Product List

Product List

Product Name	Overcharge protection voltage[V_{OV}]	Overcharge release voltage [V_{OVR}]	K	Overcharge protection delay time[t_{CD}]
IP3247AA	4.50±0.02V	4.10±0.05V	80	*
IP3247AB	4.30±0.02V	4.00±0.05V	40	*
IP3247AC	4.35±0.02V	4.05±0.05V	40	*
IP3247AD	4.40±0.02V	4.10±0.05V	40	*
IP3247AE	4.45±0.02V	4.15±0.05V	40	*
IP3247AF	4.50±0.02V	4.20±0.05V	40	*
IP3247AG	4.55±0.02V	4.25±0.05V	40	*
IP3247AH	4.60±0.02V	4.30±0.05V	40	*
IP3247AI	4.25±0.02V	4.15±0.05V	40	*
IP3247AJ	3.75±0.02V	3.60±0.05V	40	*

*Refer to chapter 9.4 for details.

8 Electrical Characteristics

Unless otherwise specified, T_A = - 40°C ~ 110°C. The Typ. Value is tested at T_A = 25°C, VDD = 14.4 V. And the Max. value and the Min. Value are tested at T_A = -40°C ~ 110°C, VDD = 6V~20V.

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
VDD and the Overvoltage Parameters						
VDD -VSS Voltage Range			6	-	20	V
VDD Quiescent Current	I_Q (VDD Current)	VC4-VC3=VC3-VC2=VC2-VC1=VC1=3.6V	-	1	2	μA
VCX Quiescent Current	I_{VCX}	VC4-VC3=VC3-VC2=VC2-VC1=VC1=3.6V	-	-	0.1	μA
Overcharge Protection Voltage	V_{OV}	T_A =25°C	V_{OV}-0.020	3.85-4.6 Step:10mV	V_{OV}+0.020	V
		T_A =0°C ~60°C	V_{OV}-0.030		V_{OV}+0.030	
		T_A =−40°C ~ +110°C	V_{OV}-0.050		V_{OV}+0.050	
Overcharge Release Voltage	V_{OVR}	T_A =25°C	V_{OVR}-0.050	3.55-4.6 Step:50mV	V_{OVR}+0.050	V
		T_A =0°C ~ +60°C	V_{OVR}-0.060		V_{OVR}+0.060	
		T_A =−40°C ~ +110°C	V_{OVR}-0.080		V_{OVR}+0.080	
OUT Output and Drive(Active High)						
OUT Output High	V_H	(VC4-VC3), (VC3-VC2), (VC2-VC1), or (VC1-GND) >V_{OV}, VDD=14.4V, I_{OH}=100μA	6	-	-	V
OUT Output Low	V_L	(VC4-VC3), (VC3-VC2), (VC2-VC1), and (VC1-GND)<V_{OV},VDD=14.4V	-	-	0.4	V
Source Current (Output High)	I_H	(VC4-VC3), (VC3-VC2), (VC2-VC1), or (VC1-GND) >V_{OV}, VDD=14.4V, CD=0V	-	-	4.5	mA
Sink Current (Output Low)	I_L	(VC4-VC3), (VC3-VC2), (VC2-VC1), and (VC1-GND)<V_{OV}, pull resistor 5k to VDD=14.4V	0.5	-	14	mA
Delay Timer						
Overvoltage Delay Time	t_{CD}	C_{CD}=100nF, K=16	1.2	1.6	2	s
Customer Test Mode Delay Time	t_{CD_TEST}	CD pin is shorted to ground	10	20	50	ms

9 Functional Description

9.1 System Diagram

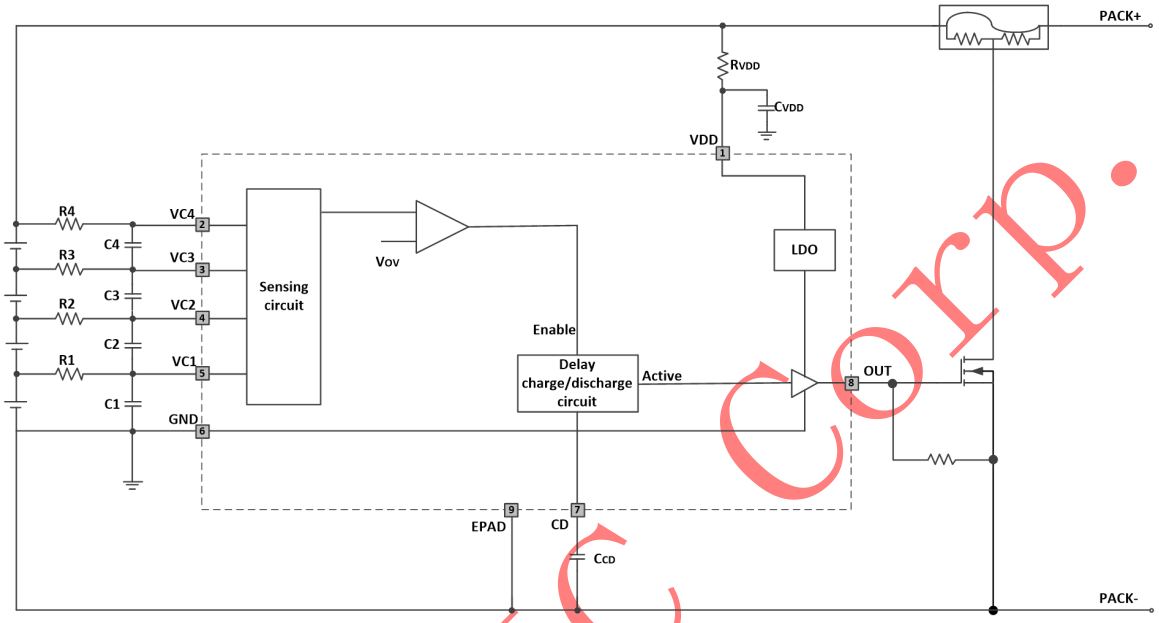


Figure 3: IP3247 Internal System Diagram

9.2 Overview

The IP3247 is an overvoltage monitor and protector for 2 to 4 series Li-Ion battery pack systems. Each cell is monitored independently for an overvoltage condition. When the IP3247 detects an overvoltage condition on any cell, the delay time is set by the free discharge time of the external capacitor on the CD pin . When the time delay expires, the overvoltage protection will be driven. If the CD pin is open circuit, short circuit or connected to a fixed level, it will be driven by the internal open circuit or short circuit fixed delay, which is the customer test mode delay.

9.3 Function Description

The IP3247 is an overvoltage monitor and protector for 2 to 4 series Li-Ion battery pack systems.If any cell voltage exceeds the programmed OV value, the Internal overvoltage timer circuit is activated and the timer circuit charges the external capacitor C_{CD} through the CD pin. When the V_{CD} voltage reaches the typical threshold value of 1.2V, it is discharged to GND slowly with a fixed current. When the V_{CD} voltage is lower than the typical threshold value of 0.2V, the OUT pin changes from low level to high level. Additionally, the internal timeout detection circuit also detects the charging time of the CD pin, to ensure that the CD pin can be charged to the 1.2V threshold successfully. If there is a timeout during charging the C_{CD} capacitor, the OUT pin will change from low level to high level. This function can be used in the customer test mode.

State change timing of Vbat (n) and OUT pin when overvoltage protection is triggered:

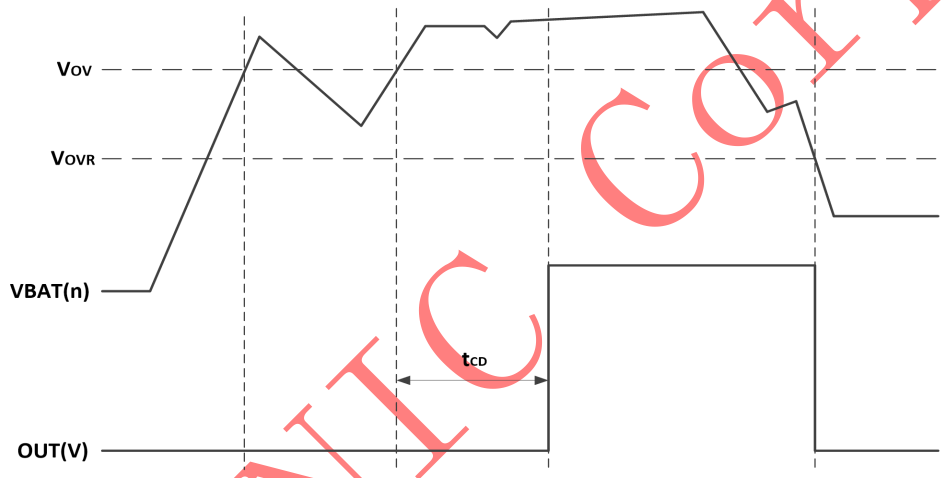


Figure4: IP3247 Overvoltage Protection Timing Chart

State change timing of CD pin when overvoltage protection is triggered:

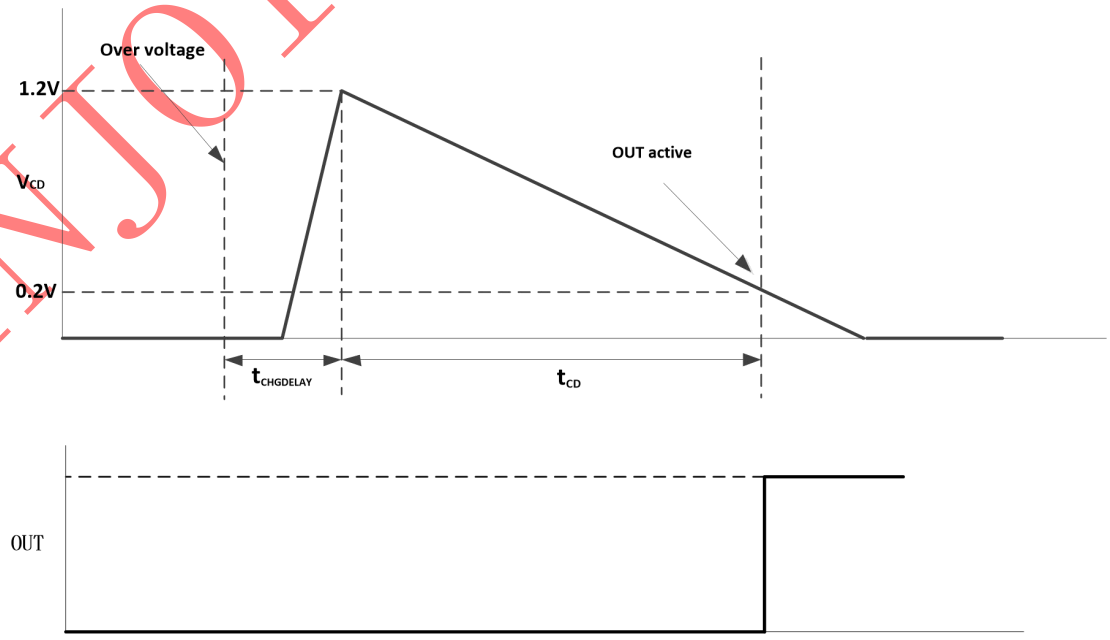


Figure 5: CD and OUT Pin Pogic When IP3247 Triggers Overvoltage Protection

Note: The maximum value of $t_{CHGDELAY}$ is 5ms and the minimum value is 1ms.

9.4 Overvoltage Protection Delay Setting

The CD pin is connected to an external capacitor that sets the delay time of overvoltage protection.When the IP3247 detects that the voltage of any cell exceeds the OV threshold, it charges the external capacitor to the voltage threshold of 1.2V through the CD pin, and then it slowly discharges the external capacitor through the delay circuit. When the voltage of the external capacitor is lower than a specific value, IP3247 activates the OUT pin and the delay ends. During charging and discharging, if the cell voltage is lower than the OV threshold, the CD pin will discharge rapidly and the IP3247 exits the timing, as shown in Fig. 4.

The relationship between the discharge delay time and the CD pin capacitor can be calculated by the following formula:

$$t_{CD} = K \times C_{CD}(\mu F)$$

Here, the C_{CD} selection range is 1nF ~ 147nF.

For example: If C_{CD} is 0.1uF and K is 16, t_{CD_MIN}=12*0.1=1.2s(Min.), $t_{CD\_TYPICAL}$=1.6s, t_{CD_MAX}=20*0.1=2s(Max.).

If the CD pin is open circuit, short circuit or connected to a fixed level, the IP3247 will enter the customer test mode, and the overvoltage delay is t_{CD_TEST}.

If the CD pin is connected with an external capacitor but the capacitor value is greater than the selection range, the IP3247 will detect timeout and enter the customer test mode.

If you want to select a long overvoltage delay, you can select a large K value. All the K value selections are shown in the following table:

Table 2: Delay Setting Coefficient K Value Selection Table

Delay Setting Coefficient K	80	40	26.5	20
	16	13.5	11.5	10
	9	8	7	6

Typical capacitor and K value are shown in the following table:

Table 3: Capacitor and K Value Selection Table of Common Delay

Delay	16ms	32ms	64ms	128ms	256ms	512ms	1s	2s	4s	8s
C_{CD}(nF)	1	2.2	4.7	10	10	47	100	100	100	100
K	16	16	13.5	13.5	25	11.5	10	20	40	80

9.5 Device Functional Modes

Normal Mode

When all of the cell voltage are below the overvoltage threshold, V_{OV}, the IP3247 operates in normal mode, and the OUT pin is at a low level.

Overvoltage Protection Mode

If any of the cell voltage exceeds the overvoltage threshold, V_{OV}, the IP3247 enters the overvoltage mode after a delay time. The OUT pin becomes high after the delay time set by the capacitor of the CD pin, and it will pull high internally. An external FET is turned on, shorting the fuse to ground, which allows the battery or charger power to blow the fuse. When all of the cell voltages fall below the V_{OVR}, the device returns to normal mode.

Customer Test Mode

The device enters the customer test mode, by opening or shorting the CD pin to GND. In this case, the OV delay will be reduced to t_{CD_TEST}, which has a maximum of 50ms.

10 Application Examples

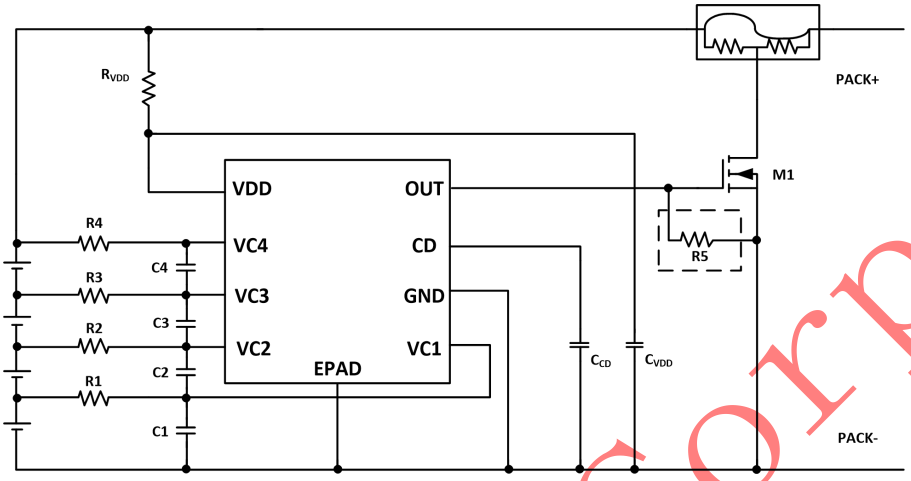


Figure 6: IP3247 Typical Application for 4-Series Cells

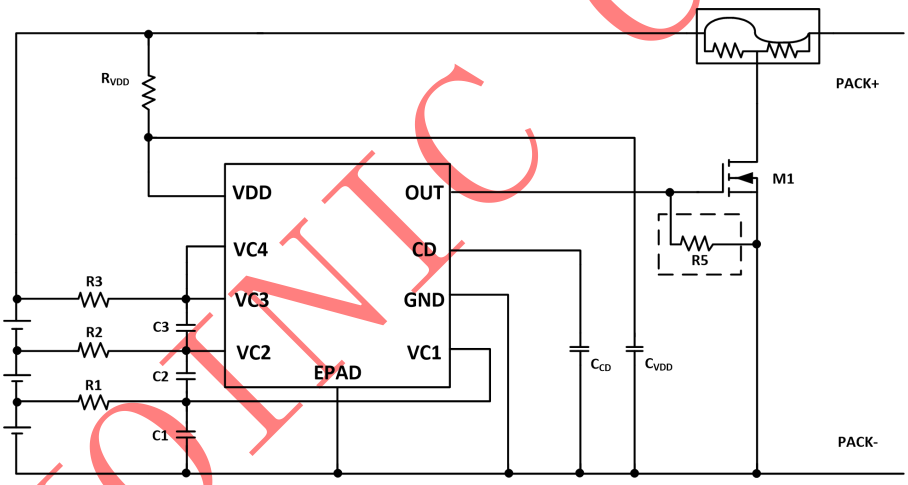


Figure 7: IP3247 Typical Application for 3-Series Cells

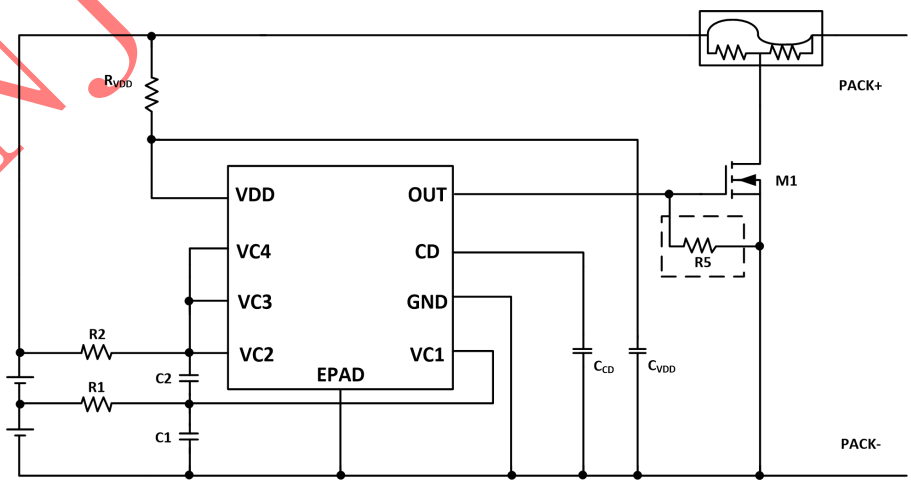


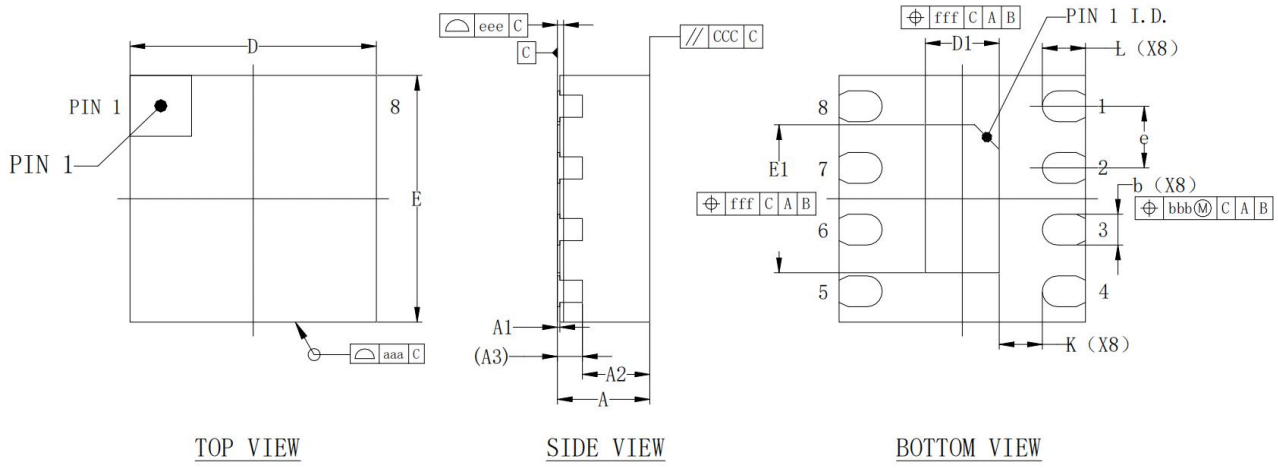
Figure 8: IP3247 Typical Application for 2-Series Cells

Table 4: Recommended Parameters of Peripheral Devices

Device	R1	R2	R3	R4	R_{VDD}	R5	M1 NMOSFET
Typ.	1kΩ	1kΩ	1kΩ	1kΩ	100Ω	4.7MΩ	-
Recommended Range	100Ω-1kΩ	100Ω-1kΩ	100Ω-1kΩ	100Ω-1kΩ	100Ω-1kΩ	3MΩ-4.7MΩ	-
Device	**C1**	**C2**	**C3**	**C4**	C_{VDD}	C_{CD}	
Typ.	0.1μF	0.1μF	0.1μF	0.1μF	0.1μF	100nF	
Recommended Range	0.1μF-1μF	0.1μF-1μF	0.1μF-1μF	0.1μF-1μF	0.1μF-1μF	1nF-147nF	

Note: Adding resistor R5 can improve the anti-interference ability of MOS, which can be increased as required.

11 Package Information



Item		Symbol	Minimum	Normal	Maximum
Body Size	X	D		2.0 BSC	
	Y	E		2.0 BSC	
Exposed Pad Size	X	D1	0.50	0.60	0.70
	Y	E1	1.10	1.20	1.30
Total Thickness		A	0.70	0.75	0.80
Stand Off		A1	0	0.02	0.05
Molding Thickness		A2		0.55	
LF Thickness		A3		0.203 REF	
Lead Width		b	0.20	0.25	0.30
Lead Length		L	0.30	0.35	0.40
Lead Pitch		e		0.50 BSC	
Lead tip to Exposed Pad		K		0.35 REF	
Package Edge Tolerance		aaa		0.10	
Lead Offset		bbb		0.10	
Molding Flatness		ccc		0.10	
Coplanarity		eee		0.05	
Exposed Pad Offset		fff		0.10	

Figure 9: IP3247 DFN8(0202)

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