

1-6 CELL Hybrid Power Synchronous Battery Charge Controller

1 Features

- Power path management:
 - Adapter and Battery Provides Power to System Together
 - ♦ Battery LEARN Function
- Input voltage range:
- Hybrid Power Boost Mode from 4.5 to 36V System
- Charge 1 to 6 Cell Battery Pack from 4.5 to 36V Adapter
- High Accuracy Power and Current Monitoring:
- ♦ ±3% Input Current Monitor Accuracy
- ♦ Comprehensive PROCHOTB profile
- ♦ ±3% Discharge Current Monitor Accuracy
- ♦ ±5% System Power Monitor Accuracy
- External setting of charging parameters
- ♦ Pin ILIM sets the charging current
- ♦ Pin INILIM sets the input current
- Select the number of cells from 1 to 6 by CELL0 to CELL2 pins
- Charge status indicator CHG_STAT and input adapter status indicator ACOK
- Supports external NTC 5-stage (JEITA) charging and the parameters are factory set
- Support 0V charging, pre-charging, fast charging, full and full charge lithium charging characteristics
- Pre-charge threshold, cut-off charge current, pre-charge current and threshold, recharge threshold, boost discharge enable and discharge status and adapter status via the status pi

voltage threshold can be set before the factory

- Protection function: input overvoltage, overcurrent, output overvoltage, overcurrent, NTC high and low temperature protection, charge timeout protection, junction temperature OTP protection
- PWM Frequency setting with SMBus register: 400kHz, 600kHz, 800kHz and MHz
- Support protection output indication
 PROCHOTB
- High precision 3.3V reference output
- Package: QFN28(0404)

2 Applications

- Notebook, Tablet PC
- Industrial and Medical Equipment
- Portable Equipment

3 Overview

IP2348 is a 1-6 cells synchronous battery charger, supports hybrid power boost mode that allows battery discharge energy to system when system power demand is temporarily higher than adapter maximum power level.

IP2348 uses two charge pumps to separately drive N-channel MOSFETs (ACFET, RBFET, and BATFET) for automatic system power source selection.

The charging and protection parameters can be flexibly configured through external pins and factory Settings to adapt to various applications. IP2348 provides feedback on the charging.







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4 Record

Note: The page numbers of previous versions may be different from those of the current version. Change page numbers for version V1.32 to V1.33 (April 2024)	Page
Modify the model description	
Added the description of electrical parameters	
Change page numbers for version V1.31 to V1.32 (February 2024)	Page
Modify the model description	
Change page numbers for version V1.30 to V1.31 (January 2025)	Page
Modify limit parameter	6
Change page numbers for version V1.20 to V1.30 (December 2024)	Page
Modify the model description	4
Change page numbers for version V1.10 to V1.20 (December 2024)	Page
Modify the model description	
Change page numbers for version V1.06 to V1.10 (October 2024)	Page
Modify the model description	4
Modify the limit parameters of CDM and HBM to 2kV	6
Modify the parameters of electrical characteristics	7
Update schematic.	
Change page numbers for version V1.05 to V1.06 (October 2024)	Page
Modified model description of IP2348_SC_3V65.	6
• Change the static power consumption when only the battery is present	7
Added on/off logic for tubes and BATFEET.	
Change page numbers for version V1.04 to V1.05 (August 2024)	Page
 Modify the crystallization temperature range 	
Change page numbers for version V1.03 to V1.04(July 2024)	Page
Add the description of common product models	
Change page numbers for version V1.02 to V1.03(June 2024)	Page
Add the description of common product models	
Delete the factory configuration options table	
Change page numbers for version V1.01 to V1.02(May 2024)	Page
 Modified the description of battery protection overvoltage delay 	
Change page numbers for version V1.00 to V1.01(April 2024)	Page
Added descriptions of common product models	
Modify datasheet format	



5 Model selection

Model name	Description
	1、The IP2348 standard product has the following specific electrical
	parameters:
	2 1. It supports charging of 1 to 6 battery strings, and the full charge voltage
	of each cell is 4.2V;
	3, 2. The number of battery strings can be set through peripheral pins, as well
	as the input current limit and charging current;
	4、3. The voltage for switching from pre-charge to constant current charging
	mode is 3V/cell (with a hysteresis of 100mV/cell), and the pre-charge current
	IS $1/10$ CC;
	5. 4. The stop charging current is $1/10$ CC, and the recharging threshold
	voltage for full charging is 97.5% CV (only LED indication, when the battery
IF2346_3TANDALONE_H	voltage output is enabled):
	6 5 The OCP protection threshold for charging and discharging is 120mV
	(the voltage on the sampling resistor) and the over-discharge voltage of the
	battery is 70% CV:
	7, 6. The NTC function is enabled, and the PWM mode operating frequency
	is 600KHz:
	8_{V} 7. There is no limit on charging timeout:
	9, 8. The charging indicator light supports lighting when the battery voltage is
	less than the recharging threshold, and the output terminal supports constant
	voltage output;
	10、The VCC overvoltage value is 40V.
	$1\sqrt{1}$ Add I2C functionality on the basis of the standard product, which can be
	used as an I2C slave device.
IP2348_SMBUS_H	2、Disable the boost discharge function.
	3、Enable the comparator, with a reference voltage of 2.3V. When the input is
	higher than the reference voltage, the output is low level.
	Based on the standard model, the following functions have been modified:
	1. The high-temperature protection threshold for NTC is set at 45° C, and the
IP2348 STANDALONE NTC H	low-temperature protection threshold is 0° C. Moreover, in the Cool and Warm
	states, the CV and CC gears are not reduced.
	2. The gear that requires maintaining a pressure difference between the input
	and output during normal operation of BUCK has been lowered.



6 Pin Configuration and Functions



Figure 2:IP2348 QFN28(0404)pin configuration

Pin	Name	I/O	Туре	Description
1	ACN	AI	Analog	Input current sense resistor positive input.
2	ACP	AI	Analog	Input current sense resistor negative input.
3	CMSRC	AO	Analog	ACDRV charge pump source input.
4	ACDRV	AI	Analog	Charge pump output to drive both ACFET and RBFET.
5	ACOK	AO	Analog	Active HIGH AC adapter detection open drain output.
6	ACDET	AI	Analog	Adapter detection input.
7	INLIM	AI	Analog	Input current setting,IAC=V _{INLIM} /(20*RAD)
8	VREF	AI	Analog	3.3V LDO output, 1uF capacitor to ground, divider resistor for NTC,INLIM,ILIM, not for other external applications
9	NTC	AI	Analog	NTC temperature sampling
10	PROCHOTB	DO	Digital	Active low, open-drain output of the processor hot indicator.
11	SDA	DIO	Digital	I2C data
12	SCL	DI	Digital	I2C clock
13	CELL0	AI	Analog	The number of batteries is set to 0
14	CELL1	AI	Analog	The number of batteries is set to 1
15	CELL2	AI	Analog	The number of batteries is set to 2
16	CHG_STAT	D	Digital	Charge status indication
17	BATSRC	AI	Analog	Connect to the source of N-channel BATFET.
18	BATDRV	AO	Analog	Charge pump output to drive N-channel MOSFET.
19	SRN	AI	Analog	Charge current sense resistor negative input.
20	SRP	AI	Analog	Charge current sense resistor positive input.
21	ILIM	AI	Analog	Charge current and discharge current limit,Small value in the charging current selector pin setting and SMBus setting, pull to GND to disable charging,ICHG=VILIM/(20*RCH).
22	GND	GND	Power	IC ground.
23	LDR	AO	Analog	Low-side power MOSFET driver output.
24	REGN	Р	Power	5.4V linear regulator output supplied from VCC.Connect a2.2-µF ceramic capacitor from REGN to GND.
25	BST	Р	Power	High-side power MOSFET driver power supply.
26	HDR	AP	Power	High-side power MOSFET driver output.
27	SW	Р	Power	High-side power MOSFET driver source.
28	VCC	Р	Power	IC input supply from adapter or battery.
Epad	GND	GND	Power	EPAD ground.



7 Absolute maximum ratings

Parameter	Symbol	Value	Unit
	BST, HDR, ACDRV, BATDRV,ACN, ACP, CMSRC, VCC, BATSRC, SW	-0.3~45	V
Voltage	ACDET, ILIM, LDR, REGN, INLIM, VREF,NTC,ACOK,CELL0,CELL1,CELL2, CHG_STATUS, PROTHOTB	-0.3~7	V
	SPR,SRN	-0.3~36	V
Differential voltage	BST-SW, HDR-SW, ACDRV-CMSRC, BATDRV-BATSRC	-0.3~7	V
Differential voltage	SRP-SRN, ACP-ACN	-0.3~0.3	V
Junction Temperature Range	TJ	-40 ~ 125	°C
Storage Temperature Range	Tstg	-60 ~ 150	°C
HBM (Human Body Model)	ESD	2	KV
CDM (Charged-Device Model)	ESD	2	KV

*Stresses beyond these listed parameter may cause permanent damage to the device.

Exposure to Absolute Maximum Rated conditions for extended periods may affect device reliability.

8 Recommended Operating Conditions

Parameter	Symbol	Min.	Тур.	Max.	Unit
	BST, HDR, ACDRV, BATDRV,SRN,SRP, ACN, ACP, CMSRC, VCC, BATSRC, SW	0		36	V
Voltage	ACDET, ISET, SDA, SCL, LDR, REGN, IADP, IDCHG, PMON,ACOK,CMPIN, CMPOUT, BATPRESB, TB_STATB,PROTHOTB	-0.3		6	V
Differential voltage	BST-SW, HDR-SW, ACDRV-CMSRC, BATDRV-BATSRC	-0.3	-	6	V
Differential voltage	TA	-40		85	°C

*Device performance cannot be guaranteed when working beyond these Recommended Operating Conditions.

 \mathcal{A}



9 Electrical Characteristics

Unless otherwise specified, 4.5 V \leq V_{vcc} \leq 36 V, -40°C \leq T_J \leq 125°C, typical value @TA=25°C.

Doromotor	Test Conditions	Range			
Parameter	Test Conditions	Min.	Тур.	Max.	it
OPERATING CONDITIONS					
V _{VCC(OP)} VCC/ACP/ACN operating voltage		4.5		36	V
CHARGE VOLTAGE REGULATION			1		
VBAT(REG_RNG) Battery voltage		1.024		26.4	V
	6cells				
	–10°C-85°C	-0.5%	25.2, 25.8,	0.5%	V
	–40°C-125°C	-0.6%	20.1, 20.4	0.6%	
	5 cells			, 	
	-10°C-85°C	-0.5%	21, 21.5	0.5%	v
	_40°C-125°C	-0.6%	21.75, 22	0.6%	
	4 cells				
	-10°C-85°C	-0.5%		0.5%	v
VBAT(REG_ACC) Charge voltage regulation accuracy	-40°C-125°C	-0.6%	17.4, 17.0	0.6%	
	3 cells		126 120		
	–10°C-85°C	-0.5%	13.05.13.2	0.5%	V
	_40°C-125°C	-0.6%	10.00,10.2	0.6%	
		0.50/	8.4, 8.6	0.50/	v
	_10 C-05 C	-0.5%	8.7, 8.8	0.5%	v
	1 cells	-0.070		0.070	
	-10°C-85°C	-0.5%	4.2, 4.3	0.5%	v
	–40°C-125°C	-0.8%	4.35, 4.4	0.8%	
CHARGE CURRENT REGULATION					
VIREG(CHG_RNG)Charge current regulationdifferentialvoltage	VIREG(CHG) = VSRP - VSRN	0		81.28	mV
	I _{CHG} =Vi∟im/(20*RCH);	-3%	4A(V _{ILIM} =0.8V)	3%	
V _{IREG(CHG_RNG)} Charge current regulationdifferentialvoltage	VILIM indicates the ILIM pin	-5%	2A(VIIIM=0.1V)	5%	mA
DISCHARGE CURRENT REGULATION	Vollage		(12111 - 7		
VIREG CHG RNG Discharge current regulation differential		0		200 50	
voltage	$V_{\text{IREG}(\text{IDISCHG})} = V_{\text{SRN}} - V_{\text{SRP}}$	0		322.50	mv
have an use Discharge outrent regulation accuracy with	I _{DCHG} =V _{ILIM} /(20*RCH);	-3%	4A(V _{ILIM} =0.8V)	3%	
10mohm RCH resistor	VILIM indicates the ILIM pin				mA
	voltage	-5%	2A (VILIM=0.1V)	5%	
INPUT CURRENT REGULATION					
VIREG_DPM_RNG Input current regulation differential voltage	VIREG DPM = VACP - VACN	0		80.64	mV
IAC_LIMIT Input current regulation accuracy with 10mohm	IAC=VINLIM/(20*RAD);	-3%	4A(VINILIM=0.8V)	3%	m
RCH resistor	voltage	-5%	2A(ViLiM=0.1V)	5%	mA
REGN/REF 参考电压	Volidgo				I
	V_{VCC} > $V_{(UVLO)}$, $V_{(ACDET)}$ >	51	54	57	V
	V(wakeup_RISE)	0.1	0.1	0.1	
	$V_{(\text{REGN})} = 0 \text{ V}, V_{\text{VCC}} > V_{(\text{UVLO})}$	80	100		mA
		3 27	2.2	3 33	µг V
VCC UNDER VOLTAGE LOCKOUT COMPARAT	OR	0.21	0.0	0.00	
$V_{VCC(UVLO)}$ Input under voltage rising threshold	-	3.6	3.8	4	V
V _{VCC(UVLO_HYS)} Input under voltage falling hysteresis			200		mV
QUIESCENT CURRENT					
IBAT Current with battery only. $T_1 = 0$ to 85°C.	V _{BAT} = 16.8 V. VCC				
I _{SRN} + I _{SRP} + I _{BATSRC} + I _{PHASE} + I _{VCC} + I _{ACP} + I _{ACN}	disconnected from battery,			5	μA
	REG0x12[15] = 1				



IP2348

		battery, vec connected nom		47	50	
-		REG0x12[15] = 1				-
		The battery consists of five to				
		from battery.		55	70	
		REG0x12[15] = 1				
		$V_{BAT} = 16.8 V$, VCC connect				
		BATEET on REG0x12[15] =				
		0, REGN = 5.4V,		700	800	
		Comparator and PROCHOTB				
		enabled, PMON				
		$V_{VCC} = 0.0000 \text{ C}$				
		$V_{(ACDET)} > 2.4 V,$		0.65	0.8	
		charge disabled				-
		$V(VCC_ULVO) < VVCC < V(ACOVP),$		16	2	
l _{AC} 适配器电流,l _{VCC} + l _{AC}	$_{\rm P}$ + $I_{\rm ACN}$ + $I_{\rm ACDRV}$ + $I_{\rm CMSRC}$	charge enabled, no switching		1.0	3	mA
		V(VCC_ULVO) < VVCC < V(ACOVP),				
		$V_{(ACDET)} > 2.4 V,$		10		
		charge enabled, switching,				
	2	MOSPET Qg 4HC				<u> </u>
		Vycc> Vycc uylo, ACDET	100	450	000	
	IE ACFET delay; V _{ACDET} > 2.4V	boost	100	150	200	ms
tacok_FALL_DEG ACOK Disat	oles the ACFET ^[GBD] delay	Vvcc> Vvcc_uvLo, ACDET buck			3	μs
	T COMPARATOR (ACOC))	0	12	15	ma
			9	12	15	1115
		Factory configuration 400kHz	340	400	460	
FswPWM switching freque	ency	Eactory configuration 600kHz	510	600	690	1
		r dotory configuration coold iz	510	000	030	
		Factory configuration 800kHz	680	800	920	KH z
		Factory configuration 800kHz Factory configuration 800kHz Factory configuration	680 850	800 1000	920 1150	KH Z
BATEET GATE DRIV	ER (BATDRV) and ACEET	Factory configuration 800kHz Factory configuration 1000kHz	680 850	800 1000	920 1150	KH z
BATFET GATE DRIV Gate drive voltage on BA	ER (BATDRV) and ACFET	Factory configuration 800kHz Factory configuration 1000kHz GATE DRIVER (ACDRV)	680 850 5.0	800 1000 5.3	920 1150 5.7	KH Z
BATFET GATE DRIV Gate drive voltage on BA RBAT(DRV OFF) BATDRV ar	ER (BATDRV) and ACFET IFET and ACFET Ind RAC(DRV OFF) ACDRV turn-off	Factory configuration 800kHz Factory configuration 800kHz Factory configuration 1000kHz GATE DRIVER (ACDRV) VBAT(DRV) – VBAT(SRC))	680 850 5.0	800 1000 5.3	920 1150 5.7	V
BATFET GATE DRIV Gate drive voltage on BA ^T R _{BAT(DRV_OFF)} BATDRV ar resistar	ER (BATDRV) and ACFET IFET and ACFET Ind RAC(DRV_OFF) ACDRV turn-off Ince	Factory configuration 800kHz Factory configuration 1000kHz GATE DRIVER (ACDRV) VBAT(DRV) – VBAT(SRC))	680 850 5.0 5	000 800 1000 5.3 6.2 6.2	920 1150 5.7 7.4	KH z V kΩ
BATFET GATE DRIV Gate drive voltage on BA R _{BAT(DRV_OFF)} BATDRV ar resistan PWM HIGH SIDE DRI	ER (BATDRV) and ACFET IFET and ACFET and RAC(DRV_OFF) ACDRV turn-off ince	Factory configuration 800kHz Factory configuration 1000kHz GATE DRIVER (ACDRV) VBAT(DRV) – VBAT(SRC))	680 850 5.0 5	800 1000 5.3 6.2	920 1150 5.7 7.4	KH z V kΩ
BATFET GATE DRIV Gate drive voltage on BA R _{BAT(DRV_OFF)} BATDRV ar resistar PWM HIGH SIDE DRI R _{DS(HI_ON)} High-side driver	ER (BATDRV) and ACFET IFET and ACFET and RAC(DRV_OFF) ACDRV turn-off ace VER (HIDRV) (HSD) turn-on resistance	Factory configuration 600kHz Factory configuration 800kHz Factory configuration 1000kHz GATE DRIVER (ACDRV) VBAT(DRV) – VBAT(SRC)) V(BTST) – V(PH) = 5.4 V	680 850 5.0 5	800 1000 5.3 6.2 6	920 1150 5.7 7.4	 KH z V kΩ Ω Ω
BATFET GATE DRIV Gate drive voltage on BA R _{BAT(DRV_OFF)} BATDRV ar resistar PWM HIGH SIDE DRI R _{DS(HI_OFF)} High-side driver R _{DS(HI_OFF)} High-side driver	ER (BATDRV) and ACFET IFET and ACFET and RAC(DRV_OFF) ACDRV turn-off ace VER (HIDRV) (HSD) turn-on resistance (HSD) turn-off Resistance refresh, comparator, threshold	Factory configuration 800kHz Factory configuration 800kHz Factory configuration 1000kHz GATE DRIVER (ACDRV) V _{BAT(DRV)} – V _{BAT(SRC)}) V _(BTST) – V _(PH) = 5.4 V V _(BTST) – V _(PH) = 5.4 V	680 850 5.0 5	800 1000 5.3 6.2 6 0.9	920 1150 5.7 7.4 10 1.4	 KH z V kΩ Ω Ω Ω
BATFET GATE DRIV Gate drive voltage on BA R _{BAT(DRV_OFF)} BATDRV ar resistan PWM HIGH SIDE DRI R _{DS(HI_OFF)} High-side driver V _{BTST_REFRESH} Bootstrap voltage	ER (BATDRV) and ACFET IFET and ACFET Ind R _{AC(DRV_OFF}) ACDRV turn-off Ince VER (HIDRV) (HSD) turn-on resistance (HSD) turn-off Resistance refresh comparator threshold	Factory configuration 600kHz Factory configuration 800kHz Factory configuration 1000kHz GATE DRIVER (ACDRV) V _{BAT(DRV)} – V _{BAT(SRC)} V _(BTST) – V _(PH) = 5.4 V V _(BTST) – V _(PH) = 5.4 V V _(BTST) – V _(PH)	5.0 5.0 3.85	800 1000 5.3 6.2 6 0.9 4.3	030 920 1150 5.7 7.4 10 1.4 4	 KH Z V kΩ Ω Ω Ω V
BATFET GATE DRIV Gate drive voltage on BA R _{BAT(DRV_OFF)} BATDRV ar resistar PWM HIGH SIDE DRI R _{DS(HI_ON)} High-side driver R _{DS(HI_OFF)} High-side driver V _{BTST_REFRESH} Bootstrap voltage PWM LOW SIDE DRI	ER (BATDRV) and ACFET IFET and ACFET and RAC(DRV_OFF) ACDRV turn-off ace VER (HIDRV) (HSD) turn-on resistance (HSD) turn-off Resistance refresh comparator threshold VER (LODRV)	Factory configuration 800kHz Factory configuration 800kHz Factory configuration 1000kHz GATE DRIVER (ACDRV) VBAT(DRV) - VBAT(SRC)) V(BTST) - V(PH) = 5.4 V V(BTST) - V(PH) = 5.4 V V(BTST) - V(PH)	5.0 5.0 5 3.85	800 1000 5.3 6.2 6 0.9 4.3	920 1150 5.7 7.4 10 1.4 4	KH z ν κΩ Ω Ω V
BATFET GATE DRIV Gate drive voltage on BA R _{BAT(DRV_OFF)} BATDRV ar resistar PWM HIGH SIDE DRI R _{DS(HI_OFF)} High-side driver V _{BTST_REFRESH} Bootstrap voltage PWM LOW SIDE DRI R _{DS(LO_ON)} Low-side driver	ER (BATDRV) and ACFET IFET and ACFET and RAC(DRV_OFF) ACDRV turn-off ace VER (HIDRV) (HSD) turn-on resistance (HSD) turn-off Resistance refresh comparator threshold VER (LODRV) (LSD) turn-on resistance	Factory configuration 600kHz Factory configuration 800kHz Factory configuration 1000kHz GATE DRIVER (ACDRV) V _{BAT(DRV)} – V _{BAT(SRC)}) $V_{(BTST)} - V_{(PH)} = 5.4 V$ $V_{(BTST)} - V_{(PH)} = 5.4 V$ $V_{(BTST)} - V_{(PH)}$	5.0 5.0 5.3.85	800 1000 5.3 6.2 6 0.9 4.3 7.5	030 920 1150 5.7 7.4 10 1.4 4 12	KH z V KΩ Ω Ω V
BATFET GATE DRIV Gate drive voltage on BA R _{BAT(DRV_OFF)} BATDRV ar resistan PWM HIGH SIDE DRI R _{DS(HI_OFF)} High-side driver V _{BTST_REFRESH} Bootstrap voltage PWM LOW SIDE DRI R _{DS(LO_ON)} Low-side driver R _{DS(LO_ONF} LOW-side driver	ER (BATDRV) and ACFET IFET and ACFET Ind R _{AC(DRV_OFF}) ACDRV turn-off Ince VER (HIDRV) (HSD) turn-on resistance (HSD) turn-off Resistance refresh comparator threshold VER (LODRV) (LSD) turn-on resistance (LSD) turn-off resistance	Factory configuration 800kHz Factory configuration 800kHz Factory configuration 1000kHz GATE DRIVER (ACDRV) $V_{BAT(DRV)} - V_{BAT(SRC)}$ $V_{(BTST)} - V_{(PH)} = 5.4 V$ $V_{(BTST)} - V_{(PH)} = 5.4 V$ $V_{(BTST)} - V_{(PH)}$	5.0 5.0 3.85	800 800 1000 5.3 6.2 6 0.9 4.3 7.5 0.75	030 920 1150 5.7 7.4 10 1.4 4 12 1.25	KH z Z KΩ Ω Ω Ω Ω Ω Ω Ω Ω
BATFET GATE DRIV Gate drive voltage on BA R _{BAT(DRV_OFF)} BATDRV ar resistar PWM HIGH SIDE DRI R _{DS(HI_OFF)} High-side driver R _{DS(HI_OFF)} High-side driver V _{BTST_REFRESH} Bootstrap voltage PWM LOW SIDE DRI R _{DS(LO_ON)} Low-side driver R _{DS(LO_OFF)} Low-side driver PROCHOTB	ER (BATDRV) and ACFET IFET and ACFET Ind R _{AC(DRV_OFF}) ACDRV turn-off ice VER (HIDRV) (HSD) turn-on resistance (HSD) turn-off Resistance refresh comparator threshold VER (LODRV) (LSD) turn-on resistance (LSD) turn-off resistance (LSD) turn-off resistance	Factory configuration 800kHz Factory configuration 800kHz Factory configuration 1000kHz GATE DRIVER (ACDRV) VBAT(DRV) – VBAT(SRC)) V(BTST) – V(PH) = 5.4 V V(BTST) – V(PH) = 5.4 V V(BTST) – V(PH)	5.0 5.0 5.0 3.85	800 800 1000 5.3 6.2 6 0.9 4.3 7.5 0.75	030 920 1150 5.7 7.4 10 1.4 4 12 1.25	KH z V kΩ Ω Ω Ω Ω Ω Ω Ω Ω Ω
BATFET GATE DRIV Gate drive voltage on BA RBAT(DRV_OFF) BATDRV ar resistar PWM HIGH SIDE DRI RDS(HI_OFF)High-side driver VBTST_REFRESH Bootstrap voltage PWM LOW SIDE DRI RDS(LO_OFF)Low-side driver RDS(LO_OFF)Low-side driver RDS(LO_OFF)Low-side driver PROCHOTB VICRITICRIT comparator th	ER (BATDRV) and ACFET IFET and ACFET and RAC(DRV_OFF) ACDRV turn-off ace VER (HIDRV) (HSD) turn-on resistance (HSD) turn-off Resistance refresh comparator threshold VER (LODRV) (LSD) turn-on resistance r(LSD) turn-off resistance r(LSD) turn-off resistance	Factory configuration 800kHz Factory configuration 800kHz Factory configuration 1000kHz GATE DRIVER (ACDRV) VBAT(DRV) - VBAT(SRC)) V(BTST) - V(PH) = 5.4 V V(BTST) - V(PH) = 5.4 V V(BTST) - V(PH) = 5.4 V V(BTST) - V(PH)	5.0 5.0 5 3.85 147% 107%	300 800 1000 5.3 6.2 6 0.9 4.3 7.5 0.75 150% 110%	030 920 1150 5.7 7.4 10 1.4 4 12 1.25 153% 112%	KH z kΩ Ω Ω Ω Ω Ω Ω Ω Ω Ω Ω Ω
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BATFET GATE DRIV Gate drive voltage on BA R _{BAT(DRV_OFF)} BATDRV ar resistar PWM HIGH SIDE DRI R _{DS(HI_ON)} High-side driver R _{DS(HI_OFF)} High-side driver V _{BTST_REFRESH} Bootstrap voltage PWM LOW SIDE DRI R _{DS(LO_ON)} Low-side driver R _{DS(LO_OFF)} Low-side driver PROCHOTB V _{ICRIT} ICRIT comparator th V _{INOM} INOM comparator th V _{VSYS} VSYS comparator th Logic input level (CEL V _{IN(HI)} Logic low level V _{IN(HI)} Logic high level LOGIC OUTPUT OPE	ER (BATDRV) and ACFET IFET and ACFET and RAC(DBV_OFF) ACDRV turn-off ace VER (HIDRV) (HSD) turn-on resistance (HSD) turn-off Resistance refresh comparator threshold VER (LODRV) (LSD) turn-on resistance (LSD) turn-off resistance (LSD) turn-off resistance reshold reshold treshold top,CELL1,CELL2)	Factory configuration 800kHz Factory configuration 800kHz Factory configuration 1000kHz GATE DRIVER (ACDRV) VBAT(DRV) - VBAT(SRC)) V(BTST) - V(PH) = 5.4 V V(BTST) - V(PH) = 5.4 V V(BTST) - V(PH) = 5.4 V V(BTST) - V(PH) State ATD 5 m 4 drain oursant	510 680 850 5.0 5 3.85 147% 107% 5.88 2.1	800 800 1000 5.3 6.2 6 0.9 4.3 7.5 0.75 150% 110% 6	030 920 1150 5.7 7.4 10 1.4 4 12 1.25 153% 112% 6.12 0.8	KH z κΩ Ω Ω Ω Ω Ω Ω Υ Ν Υ Υ Υ Ν Υ
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IP2348

							_
	VNTC_HOT_TH_HSY	VNTC REG08 corres 5°C	rises, 3<2:1>=00, ponding to temperature		3.25		%
	V _{NTC_WT_TH}	VNTC to a te	drops, corresponding mperature of 45°C	42.7	44.7	46.7	%
	VNTC_WT_TH_HSY	VNTC a temp	rises, corresponding to perature of 5°C		3.75		%
	VNTC_COOL_TH COTTEN 10°C		rises, REG08<0>=0, ponding to temperature	66.25	68.25	70.3	%
	VNTC_COOL_TH_HSY	VNTC to a te	drops, corresponding mperature of 5°C		3		%
	VNTC_COLD_TH	VNTC a temp	rises, corresponding to erature of 0°C	71.25	73.25	75.3	%
	VNTC_COLD_TH_HSY	VNTC to a te	drops, corresponding mperature of 5°C		2.5		%
Input Overvoltage C	omparator (ACOVP)			•			
V(ACOV)VCC overvoltage	threshold (ACOVP gear pin sele	ct 6.4V)	VCC boost voltage		6.30		
V(ACOV) VCC overvoltage threshold (ACOVP gear pin select 17.6V)		t 17.6V)	VCC boost voltage		17.26		
V(ACOV)VCC overvoltage threshold (ACOVP gear pin select 24V)		ct 24V)	VCC boost voltage		23.46		
V _(ACOV) VCC overvoltage threshold (ACOVP gear pin select 30.4V)		t 30.4V)	VCC boost voltage		29.65		
V(ACOV)VCC overvoltage	threshold (ACOVP gear pin sele	ct 40V)	VCC boost voltage		38.83		
V _(ACOV_HYS) V	/CC overvoltage hysteresis		VCC depressurization		0.85		



10 FUNCTIONAL DESCRIPTION

10.1 System Diagram





10.2 Overview

IP2348 is a 1-6 cells synchronous battery charger, supports hybrid power boost mode that allows battery discharge energy to system when system power demand is temporarily higher than adapter maximum power level.

IP2348 uses two charge pumps to separately drive N-channel MOSFETs (ACFET, RBFET, and BATFET) for automatic system power source selection.

Through SMBus, system power management micro controller programs input current, charge current, discharge current, and charge voltage with high regulation accuracies.

The charging and protection parameters can be flexibly configured through external pins and factory Settings to adapt to various applications. The IP2348 provides feedback on the charging status and adapter status via the status pin.

10.3 System power

10.3.1 System power

The IP2348 gets power from VCC. After VCC is above its UVLO threshold, the device wakes up, REGN is enabled when VCC present, and power for digital and analog block inside.

If power path latches off, VCC input is the higher voltage between adapter and battery through an external diode, if battery only, IP2348 stays in low power mode with lowest quiescent current(50uA typical),BFET driver enabled. If power path latch off is disabled, VCC only connect to the adapter.

10.3.2 Adapter Detect and ACOK Output

The device detect adapter through AC_DET pin. ACOK is enable if the adapter is present, and the charge pump drivers of ACFET and RBFET both work. If the adapter does not exist, ACFET and RBFET are off and BATFET is on. The switching logic is to turn on the MOS tube that needs to work when the MOS tube V_{GS} is less than 100us of 3V.

10.3.3 Battery Only

When only the battery is present, the battery supplies power to the VCC and enters the low-power mode. Only the UVLO module and digital module of the VCC are enabled. The power consumption is controlled at 70uA and the REGN LDO is 0. If the path management function is not included, the VCC is not connected to the battery. When the adapter is removed, the battery consumption is less than 5uA.

10.4Adapter Detect, ACOK and Adapter Overvoltage (ACOVP)

10.4.1 ACDET

Program adapter valid input voltage threshold by connecting a resistor divider from adapter input to ACDET pin. When ACDET is above 2.4V, and VCC is above SRN but below ACOV, ACOK goes HIGH. **10.4.2 ACOK**

The open drain ACOK output can be pulled to external rail under the following conditions:

- 1. V_{ACDET}>2.4V
- 2. V_{VCC_UVLO}<VCC<ACOVP
- 3. VCC- VSRN>V_{VCC_SRN_FALL}+V_{VCC_SRN_HYST} (The pressure difference that needs to be maintained depends on the value 0X32[1])

Such as: $\buildrel 0x32[1]=0$, VSRN=12.8V, VCC-VSRN>260mV; 0x32[1]=1, VCC-VSRN>1.47V. If any of the above conditions are not met, it is considered that the adapter is not present, ACOK is



pulled low, and charging is disabled. ACFET/RBFET are turned off to disconnect the adapter to system. BATFET is turned on if turn-on conditions are valid.

10.4.3 ACOVP

ACOVP is threshold is divided into five gears, according to the VCC voltage 6.4 V, 17.6 V, 24 V, 30.4 V, 40 V, hysteresis of 0.85 V. During ACOVP, ACFET and RBFET are turned off, BATFET is turned on (to meet battery voltage supply), system power is battery powered and VAC overvoltage protection is released when the VAC returns below the overvoltage recovery value.

10.5 Processor Hot Indication

The PROCHOTB triggering events include:

- ICRIT: adapter peak current
- INOM: adapter average current (110% of input current limit)
- IDCHG: battery discharge current
- VSYS: system voltage on SRN lower than 6V for 2s 6s battery
- ACOK: upon adapter removal (ACOK pin HIGH to LOW)
- BATPRES: upon battery removal (BATPRES pin LOW to HIGH)
- CMPOUT: Independent comparator output (CMPOUT pin HIGH to LOW).

10.6 DCM

If the average inductor current below 125 mA (on 10 mohm), the converter enters DCM mode, if the average inductor current above 250mA(on 10mohm), the converter enters CCM mode.

10.7 Protection

10.7.1 Input Overcurrent Protection (ACOC)

When the input current exceeds 1.25x or 2x of ICRIT set point (with 12-ms deglitch time), ACFET/RBFET is latches off and an adapter removal is required to force ACDET < 0.6 V to reset IC. After IC reset from latch off, ACFET/RBFET can be turned on again. The ACOC function threshold can be set or disabled through REG0x37 [10:9].

10.7.2 Charge Overcurrent Protection (CHGOCP)

IP2348 has cycle-by-cycle peak overcurrent protection. It monitors the voltage across SRP and SRN, and prevents the current from exceeding the threshold based on the charge current set point. The high-side gate drive turns off for the rest of the cycle when over current is detected, and resumes when the next cycle starts. The charge OCP threshold can be set through REG0x35[2:1].

10.7.3 Battery Overvoltage Protection (BATOVP)

IP2348 does not allow the high-side and low-side MOSFET to turn-on when the battery voltage at SRN exceeds 104% of the regulation voltage set point. Charger is completely disabled.

10.7.4 Battery Short

When battery voltage on SRN falls below 2.4 V, the converter begins to pulse charging with 200ns turns on and period can be setting by registers.

10.7.5 Input over-voltage and UVLO

Input overvoltage protection occurs when the input VCC exceeds the set overvoltage value. Input undervoltage protection is triggered when the input VCC UVLO threshold is lower. No charge occurs after input overvoltage and undervoltage protection, and both ACFET and RBFET are turned off.



10.8 Hybrid Power Boost Mode

IP2348 supports the hybrid power boost mode by allowing battery discharge energy to system when system power demand is temporarily higher than adapter maximum power level.

Hybrid power boosts mode setting:

- Whether to enable or not can be factory selected Settings;
- Input current is higher than 107% of input current limit;
- Discharge current depends on system current requirement and adapter current limit
- The boost voltage is equal to system voltage

• Boost Discharge current exceeds the set limit. The system current continues to increase. The input current exceeds a certain threshold, and the output protection state is PROCHOTB, reminding the system to reduce the power.

10.9 Charge

IP2348 supports the typical charging mode and typical charging process of lithium batteries. For deeply discharged batteries whose terminal voltage is below the pre-charge threshold ($V_{LOW_TH}*N$), the IP2348 will start precharging with a precharge Current. When the battery voltage reaches the pre-threshold, the chip starts charging with a constant current at the current value set by the ILIM pin. Once the battery voltage reaches the set CV value, the chip will operate in constant voltage (CV) mode until the battery is fully charged. In CV mode, the charging current drops and stops charging when the charging current in CV mode drops to EOC current.



IP2348 can set the end of charge threshold (EOC) current. When entering the charging process in CV mode, the charging current will gradually drop to the end of charge current threshold, and the chip will stop charging. When the battery voltage is lower than the set recharging threshold, the chip automatically restarts to charge.

CC can be set by ILIM pin, CV, EOC, precharge threshold, recharge threshold can be set by factory configuration, charging status can be displayed by CHG_STAT. Input current limit is set by external pin INILIM, and battery node number can be selected by internal factory or external pin.



10.9.1 Precharge

Precharge threshold setting:

Precharge/quick charge threshold can be factory selected 2.8V or 3V per section, default is 3V; Precharge current setting:

Precharge current can be factory selected 1/10 CC current value or 1/5 CC current value, default is 1/10 CC.

10.9.2 CC, CV, input current limiting settings

CC, IAC by pin ILIM, IINLIM set:

ILIM pin set formula: ICG = VILIM / (20 * RCH), VILIM by REF through the voltage divider set; IINLIM set formula: IAC = VINLIM / (20 * RAD), VINLIM by REF through the voltage divider set. CV by register set single section CV voltage, section number by CELLx pin set:

single cell CV fixed voltage: 4.2V/CELL, 4.3V/CELL, 4.35V/CELL, 4.4V/CELL;

battery section number can be set by internal or external pin selection (CELL0, CELL1, CELL2), external setting method is:

PIN	LOGIC							
CELL2	L	L	L	L	Н	Ŧ	Н	Н
CELL1	L	L	Н	Н	L	L	Н	Н
CELL0	L	Н	L	Н	L	Н	L	Н
CELLS SET	1CELL	2CELL	3CELL	4CELL	5CELL	6CELL	6CELL	6CELL

10.9.3Full charge and recharge

When the charging current in CV stage is reduced below the full charge current, the battery is considered to have been charged, and the threshold of full charge current is 1/20 CC or 1/10 CC, which is set by the factory and defaults to 1/20 CC current.

The recharge voltage threshold can be set from the factory to 97.5% CV or 95% CV.

10.9.4 Time out

Charging timer counts the charging time, including a pre-charging charging timer and a fast charging timer. When the timer times out and triggers, the charging stops. The charging conditions are as follows: reinsert the adapter and reinsert the battery. The charging timer can be factory set to disable or enable, and the timer time can also be factory set. The details are as follows:

	-	
Options	Precharge time	Fast charge (CC+CV) time
1	disable	disable
2	30m	4h
3	1h	8h
4	2h	16h

10.9.5 NTC sampling and 5-stage JEITA charging standard

IP2348 has a negative temperature coefficient (NTC) resistance to detect battery temperature and enable JEITA standard charging. When the battery temperature rises to the hot threshold VNTC_HOT_TH or decreases to the cold threshold VNTC_COLD_TH, the chip will turn off the charging function. When the battery temperature rises between the warm threshold VNTC_WT_TH and the hot threshold VNTC_HOT_TH, the CV voltage can be reduced according to the factory configuration. When the battery temperature is between



the cool threshold VNTC_COOL_TH and the cold threshold VNTC_COLD_TH, CV and CC are reduced according to the factory Settings. The NTC function and parameters can be disabled by factory Settings. VNTC_WT_TH and VNTC_COLD_TH correspond to temperatures of 45°C and 0°C, respectively.5 段式 JEITA 充电标准 As shown in Figure 5 below:



Figure 5: JEITA charging diagram

The NTC principle of the following figure is shown in Figure 6, where the NTC resistance is selected NCP18XH103, B25/50=3380K, and the values of RT1 and RT2 can be determined using the following formula:

$$RT2 = \frac{V_{IN} \times RTH_{COLD} \times RTH_{HOT} \times \left(\frac{1}{VT1} - \frac{1}{VT5}\right)}{RTH_{HOT} \times \left(\frac{V_{IN}}{VT5} - 1\right) - RTH_{COLD} \times \left(\frac{V_{IN}}{VT1} - 1\right)}$$
$$RT1 = \frac{\left(\frac{V_{IN}}{VT1} - 1\right)}{\frac{1}{RT2} + \frac{1}{RTH_{COLD}}}$$

Select 60°C as the Hot temperature, R_{THCOLD} = 27.22 k Ω , R_{THHOT} = 3.01k Ω VT1=73.25% x VIN, VT5=34.37% x VIN, RT2=30.18k Ω , RT1=5.23k Ω



Figure 6:principles of NTC setting

10.9.6 Charging status indicates CHG_STAT

CHG_STAT is the open leakage output. When charging, CHG_STAT is low and the external LED is on. When charging is complete, CHG_STAT output high resistance, LED off; When charge protection occurs, including NTC high and low temperature protection, charge timeout, etc., CHG_STAT outputs square waves at 1Hz, 50% duty cycle, and the LED light flashes.



10.9.7 Enable and Disable Charging

Charging Enable:

- ACOK is active high
- ILIM pin voltage is higher than 100 mV
- Not in protection state(including battery OVP, junction temperature protection, input over-current protection

Charging disable:

- ILIM pin voltage is lower than 60 mV
- ACOK is pulled low
- In protection state(including battery OVP, junction temperature protection, input over-current protection)



11 Typical Application Circuit



Figure 7: IP2348 Typical Application Circuit



IP2348

12 Package Information



Figure 8: QFN28 (0404)



13 IC IC Silk-screen Information



V1.30



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